Application Note

fast SiC semiconductor

AN-001

SiC MOSFET Clamped Inductive Load Switching Evaluation Kit

FSSEVB_CILS Rev. C
FFSEVB_GDrv Rev. E

fast SiC semiconductor Inc.
Hsinchu, Taiwan

CAUTION

PLEASE CAREFULLY REVIEW THE FOLLOWING PAGES, AS THEY CONTAIN IMPORTANT INFORMATION REGARDING THE HAZARDS AND SAFE OPERATING REQUIREMENTS RELATED TO THE HANDLING AND USE OF THIS BOARD.

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD. THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS EVALUATION BOARD WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS BOARD CAN REACH TEMPERATURES ABOVE 50˚ CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE FOR A SHORT TIME AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED.

Please ensure that appropriate safety procedures are followed when operating this board, as any of the following can occur if you handle or use this board without following proper safety precautions:

- **Death**
- **Serious injury**
- **Electrocution**
- **Electrical shock**
- **Electrical burns**
- **Severe heat burns**

You must read this document in its entirety before operating this board. It is not necessary for you to touch the board while it is energized. All test and measurement probes or attachments must be attached before the board is energized. You must never leave this board unattended or handle it when energized, and you must always ensure that all bulk capacitors have completely discharged prior to handling the board. Do not change the devices to be tested until the board is disconnected from the electrical source and the bulk capacitors have fully discharged.

This document is prepared as a reference to install and operate Fast SiC Semiconductor Inc. evaluation hardware.

All parts of this application note are provided in English. If the end user of this board is not fluent in any of these languages, it is your responsibility to ensure that they understand the terms and conditions described in this document, including without limitation the hazards of and safe operating conditions for this board.

Note: This FSS-designed evaluation hardware for Fast SiC Semiconductor Inc. components is a fragile, high voltage, high temperature power electronics system that is meant to be used as an evaluation tool in a lab setting and to be handled and operated by highly qualified technicians or engineers. When this hardware is not in use, it should be stored in an area that has a storage temperature ranging from -40˚ Celsius to 150˚ Celsius and if this hardware is transported, special care should be taken during transportation to avoid damaging the board or its fragile components and the board should be transported carefully in an electrostatic discharge (ESD) bag to avoid any damage to electronic components. The hardware does not contain any hazardous substances, is not designed to meet any industrial, technical, or safety standards or classifications, and is not a production qualified assembly.

0. Manu

1. Introduction:

SiC MOSFET Clamped Inductive Load Switching Evaluation Kit

1.1 Feature

To demonstrate the high performance under clamped inductive load switching of Fast SiC semiconductor Inc. (abbreviated as "FSS") MOSFETs with a gate driving daughter board and a clamped inductive load carrier board, this evaluation board and application note be established. This evaluation board (Fig. 1) comes configured as a half-bridge but it can be configured into other common topologies such as a conventional / synchronous boost or conventional / synchronous buck topology.

This board was designed to:

- Evaluate the inductive and resistive switching performance and characterize E_{ON}, E_{OFF}, t_{ON}, t_{OFF}, Q_{rr}, or other related dynamic behaviors in FSS SiC MOSFETs.
- Evaluate SiC MOSFET steady-state performance. The bare copper with electroless nickel immersion gold pad-opening on the bottom of the PCB with multi-through holes directly connected to the lead frame of power MOSFET(1). To measure the case temperature of SiC MOSFETs, users could setup thermocouples on the bottom copper so the temperature just underneath the MOSFET's case can be measured.
- Evaluate the operated ruggedness and characterize the dv/dt ruggedness, the single-pulsed avalanche energy, the repetitive avalanche energy, the safe operation area, and the short-circuit withstanding time.(2)
- Evaluate the SiC MOSFETs under practical applications such as buck converter, boost converter, half-bridge converter, and/or other topologies.
- Referenced as a layout example for driving SiC MOSFETs.
- Use as a test platform to evaluate and tune the gate driver circuitry for FSS SiC MOSFETs.

(1) FSS is working hard to realize a high speed driver board in a limited space and FR-4 material to control the cost-performance balance and convenience-to-use. However, please also recognized that there is still a temperature difference between the lead frame and the bottom copper layer with gate driving daughter boards.

2) When using as a ruggedness test platform, the over-stress condition such as over voltage and over current may occur. For users' safety, the users are highly recommended to discuss with FSS's technical support specialists.

1.2 Electrical Specifications

Items	Electrical Spec.
Max. DC-Bus Voltage	800V
Max isolated Voltage (power-signal)	2.5 kV_{rms}
Max. DC Current	15A
Vcc	5V
Input Signal	2.5V to 5V logic
UVLO	12V
Propagation Delay (PWM)	< 60nsec
Bleeding Time	< 1sec@ 500V

1.3 Ordering Information

Part Number	Description
FSSEVB_CILS	Clamped Inductive Load Carrier
FSSEVB_GDrv	Gate Driving Daughter Board
FF06190A	Falcon Series – SiC MOSFET

For further information about comparable products, please contact (www.fastsic.com).

1.4 Kit Overview

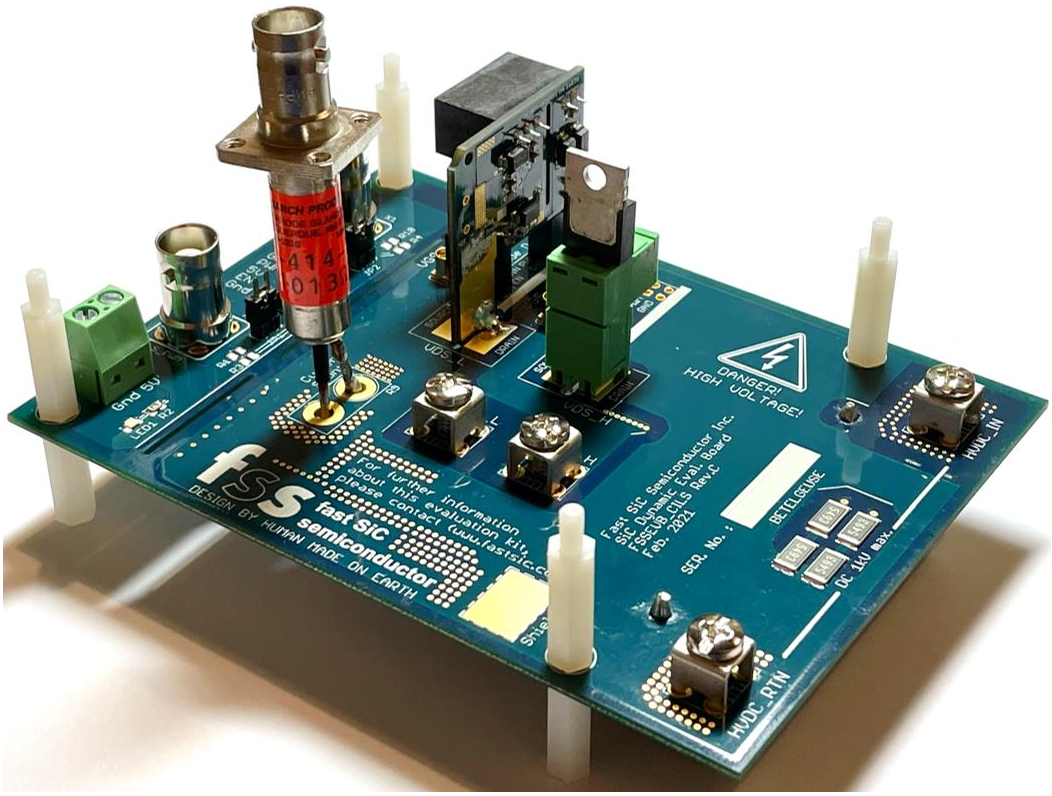

Fig. 1. FSSEVB_CILS Evaluation Kit

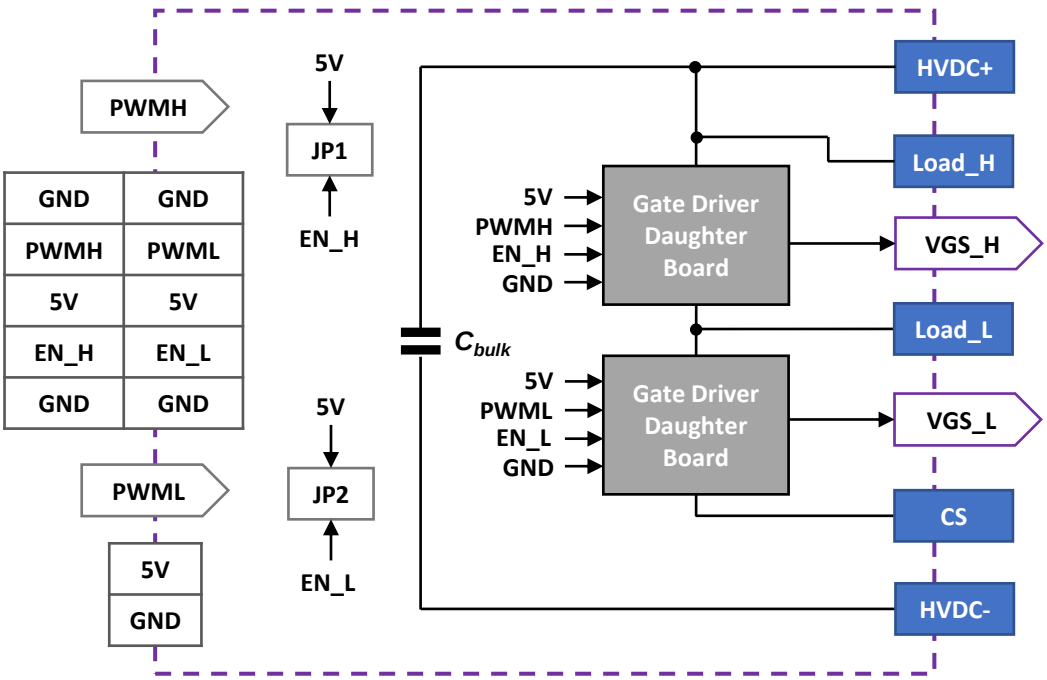

Fig. 2. Block Diagram of FSSEVB_CILS Evaluation Kit

Fig. 3. FSSEVB_GDrv Daughter Board

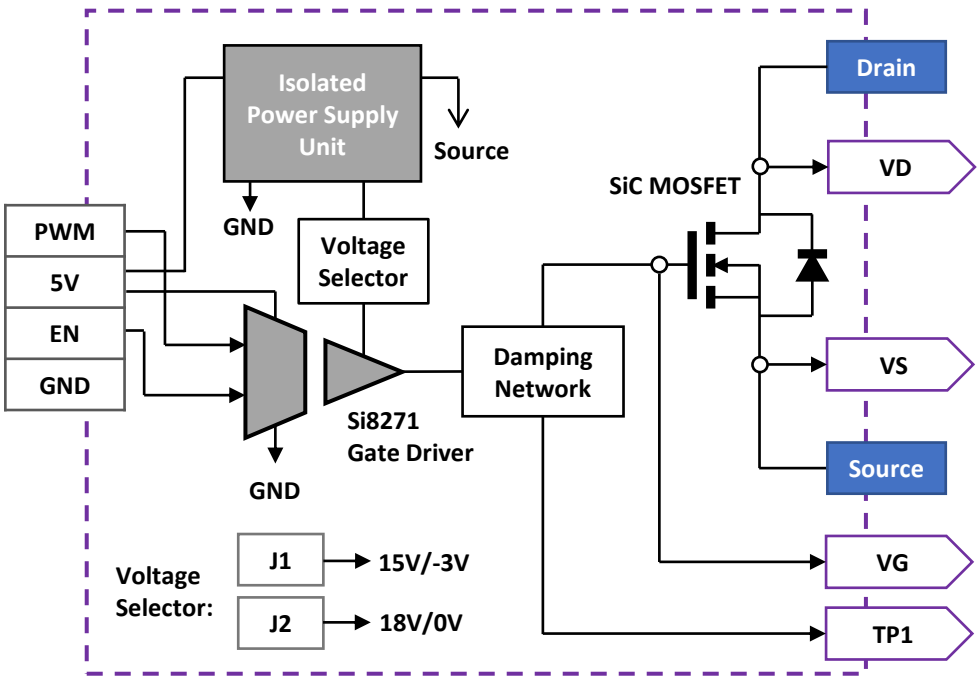

Fig. 4. Block Diagram of FSSEVB_GDrv Daughter Board

2. Functional Description:

2.1 Operating Range

The maximum rating and recommended operated electrical rating of this evaluation are demonstrated in the table below, FSS can **NOT** guarantee the safety and availability to any over-driving conditions.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Driving Daughter Board						
Standard Operating Conditions						
Auxiliary Power Input	V_{AUX}	4.5	5	5.5	V	
Auxiliary Power Start-up Time	$T_{ON, AUX}$		30		µs	
Max. Auxiliary Power Output	$P_{out, AUX}$	--	--	2	W	
Max. Operated Temperature	T_{max}	-40	--	85	˚C	Limited by DC/DC Converter
Build-in Turn-on Gate Resistance	R_{GG_on}	--	2.7	--	Ω	
Build-in Turn-off Gate Resistance	R_{GG_off}	--	1	--		
Turn-on Peak Source Current	I_{GG_on}	--	1.5	--	A	t_{peak} < 250ns
Turn-on Peak Sink Current	I_{GG_off}	--	3.3	--		
Undervoltage Lockout (UVLO)						
V_{AUX} UVLO Positive Threshold	$V_{AUX, UV+}$	1.85	2.20	2.45	V	
V_{AUX} UVLO Negative Threshold	$V_{AUX, UV-}$	1.75	2.1	2.35		
Gate Driver Output UVLO Positive Threshold	$V_{DD, UV+}$	11	12.2	13.5		
Gate Driver Output UVLO Negative Threshold	$V_{DD, UV-}$	9.6	10.8	12.1		
Digital Signal						
Digita High Input Threshold	$V_{Digital+}$	2.0	--	--	V	
Digita Low Input Threshold	$V_{Digital-}$	--	--	0.8		
Digita Input Hysteresis	$V_{Dig, hys.}$	350	400	--	mV	
AC Parameters						
Propagation Delay	t_{PHL}, t_{PLH}	30	45	75	ns	C_L = 200 pF
Pulse Width Distortion	PWD	--	38	47		$\lvert t_{PLH} - t_{PHL} \rvert$
Gate Output Rise Time	$t_{r, gate}$	4	10.5	16		C_L = 200 pF
Gate Output Fall Time	$t_{f, gate}$	5.5	13.3	18		
Shutdown Time from Enable False	t_{SD}	--	--	60		
Restart Time from Enable True	$t_{RESTART}$	--	--	60		
Common Mode Transient Immunity	CMTI	200k	350k	400k	V/µs	V_{CM}=1500V
Clamped Inductive Load Carrier						
DC-Bus Voltage	V_{DC-bus}			800	V	
Bleeding Time	t_{bleed}		650		msec	V_{DC-bus}=500V
Maximum DC Current	I_{DC}			15	A	

2.2 Signal Control Behavior

2.2.1 Undervoltage Lockout Operation

Device behavior during start-up, normal operation, and shutdown are shown in the figure below, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. UVLO is provided to prevent erroneous operation during the gate drive IC startup and shutdown or when V_{DD} is below its specified operating circuit range. Noted that the input (control) side and Driver have their own undervoltage lockout monitors.

The UVLO circuit unconditionally drives V_{GG} low when V_{DD} is below the lockout threshold. Upon power-up, the gate driver is maintained in UVLO until V_{DD} rises above $V_{DD,\ UV+}$. During power-down, the gate driver enters UVLO when V_{DD} falls below the UVLO threshold plus hysteresis. Please refer to page 7 for UVLO values.

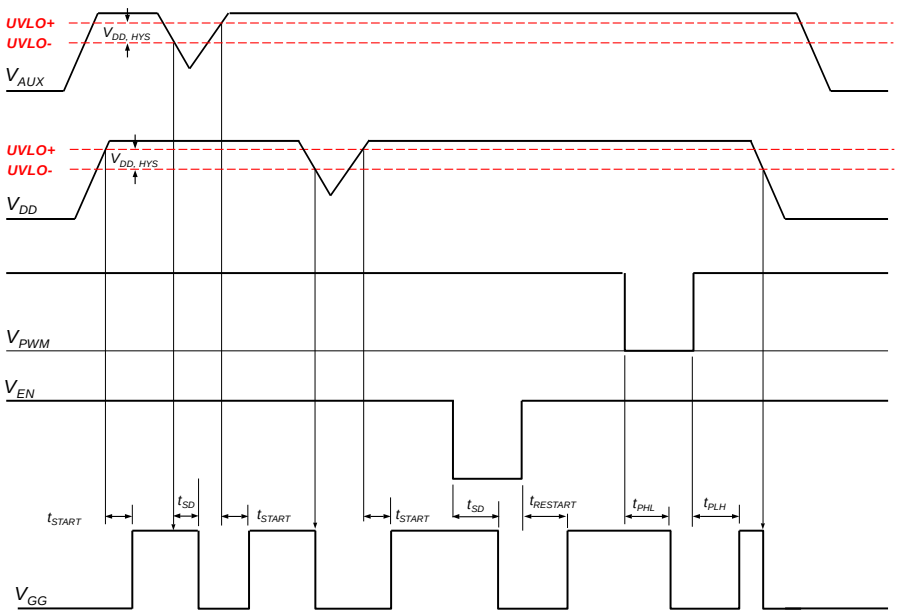

Fig. 5. Device Behavior during Normal Operation and Shutdown

2.2.2 Control Inputs

PWM input is high-true, TTL level-compatible logic inputs. A logic high signal on PWM input causes the corresponding output to go high.

2.2.3 Enable Inputs

When brought low, the ENABLE input unconditionally drives V_{GG} low regardless of the states of PWM_{in}. Device operation terminates within t_{SD} after $V_{EN} = V_{digital-}$ and resumes within $t_{RESTART}$ after $V_{EN} = V_{digital+}$. The ENABLE input has no effect if V_{DD} is below its UVLO level.

2.2.4 Truth Table

The truth table of the embedded gate driver IC is recorded below.

Truth Table					
Inputs	V_{DD} State	V_{EN}	Output		Note
V_{PWM}			V_{GG+}	V_{GG-}	
L	Powered	H	Hi-Z	L	This truth table assumes VDDA and VDDB of the driver IC are powered. If VDDA and VDDB are below UVLO, see the next page for more information. An input can power the input die through an internal diode if its source has adequate current.
H	Powered	H	H	Hi-Z	
X	Non-Powered	X	Hi-Z	L	
X	Powered	L	Hi-Z	L	

2.3 Critical Board Instruction

2.3.1 Overview

To evaluate FSS SiC MOSFET on this evaluation kit, the important ports, connectors, and components are highlighted below:

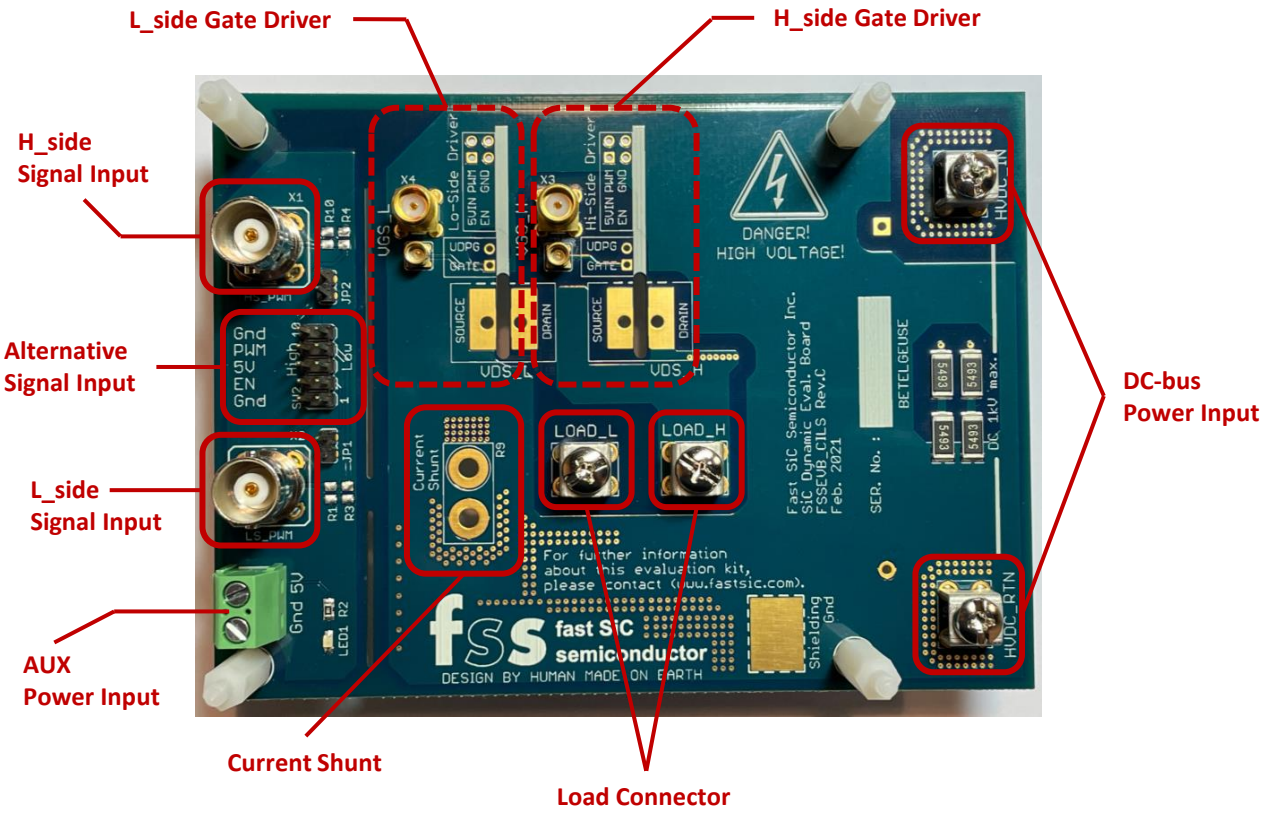

Fig. 6. Overview of FSSEVB_CILS Evaluation Kit

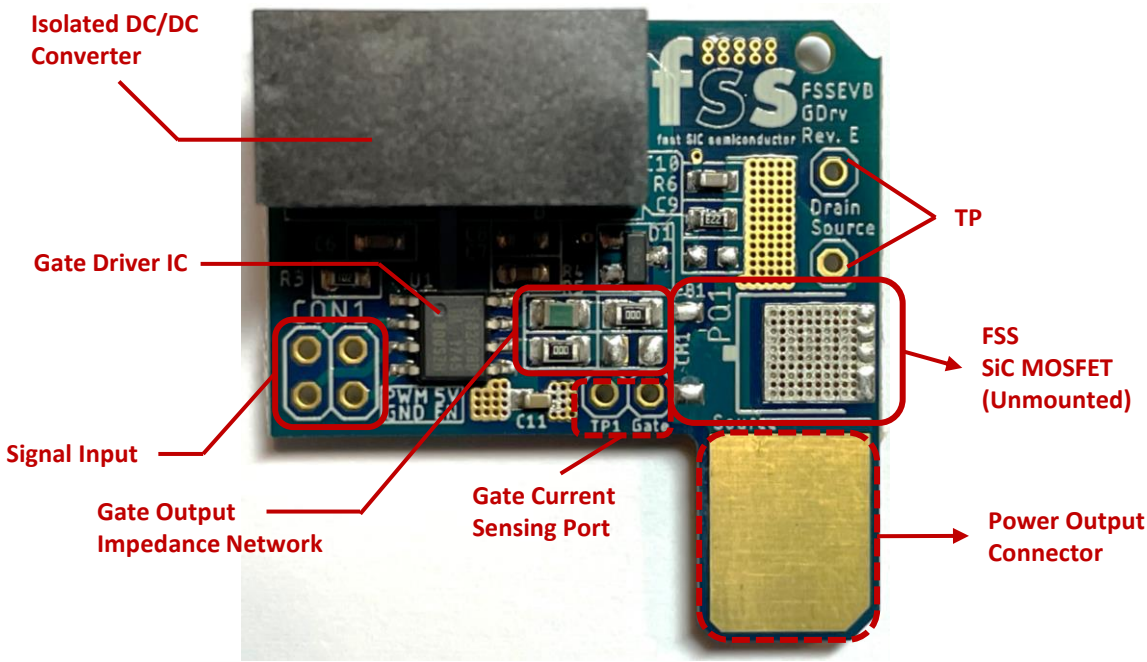

Fig. 7. Overview of FSSEVB_GDrv Daughter Board

2.3.2 Control Signal Input

The critical control signal input ports on the FSSEVB_CILS evaluation kit are shown below:

- X1 is a BNC connector with 50Ω of impedance. As a control of the H_side PWM input of the related gate driver in a half-bridge topology, X1 is also short with the PWM pin in SV2, the alternative H_side signal input port, for the convenience of directly implement the MCU's control signals.
- X2 is a BNC connector with 50Ω of impedance. As a control of the L_side PWM input of the related gate driver in a half-bridge topology, X2 is also short with the PWM pin in SV2, the alternative L_side signal input port, for the convenience of directly implement the MCU's control signals.
- JP1 is a jumper of L_side to select whether the enable pin is connected with the AUX 5V input pin or make them independent. To enable the related gate drivers, JP1 is default shorted. Therefore the drivers are always enabled while the AUX power is active. For further signal manipulating or other specific tests, users could remove the jumper and manipulate the enable signal by themselves.
- JP2 is a jumper of H_side to select whether the enable pin is connected with the AUX 5V input pin or make them independent. To enable the related gate drivers, JP2 is default shorted. Therefore the drivers are always enabled while the AUX power is active. For further signal manipulating or other specific tests, users could remove the jumper and manipulate the enable signal by themselves.
- The AUX Power input port is the auxiliary power supply for all the signal control stage and the gate driver boards. Typically, the preferred input voltage is 5V.

Moreover, the signal input port CON1 of the FSSEVB_GDrv board is typically mounted on the FSSEVB_CILS kit and connected with the high side/ low side signal ports, as Fig. 8 described.

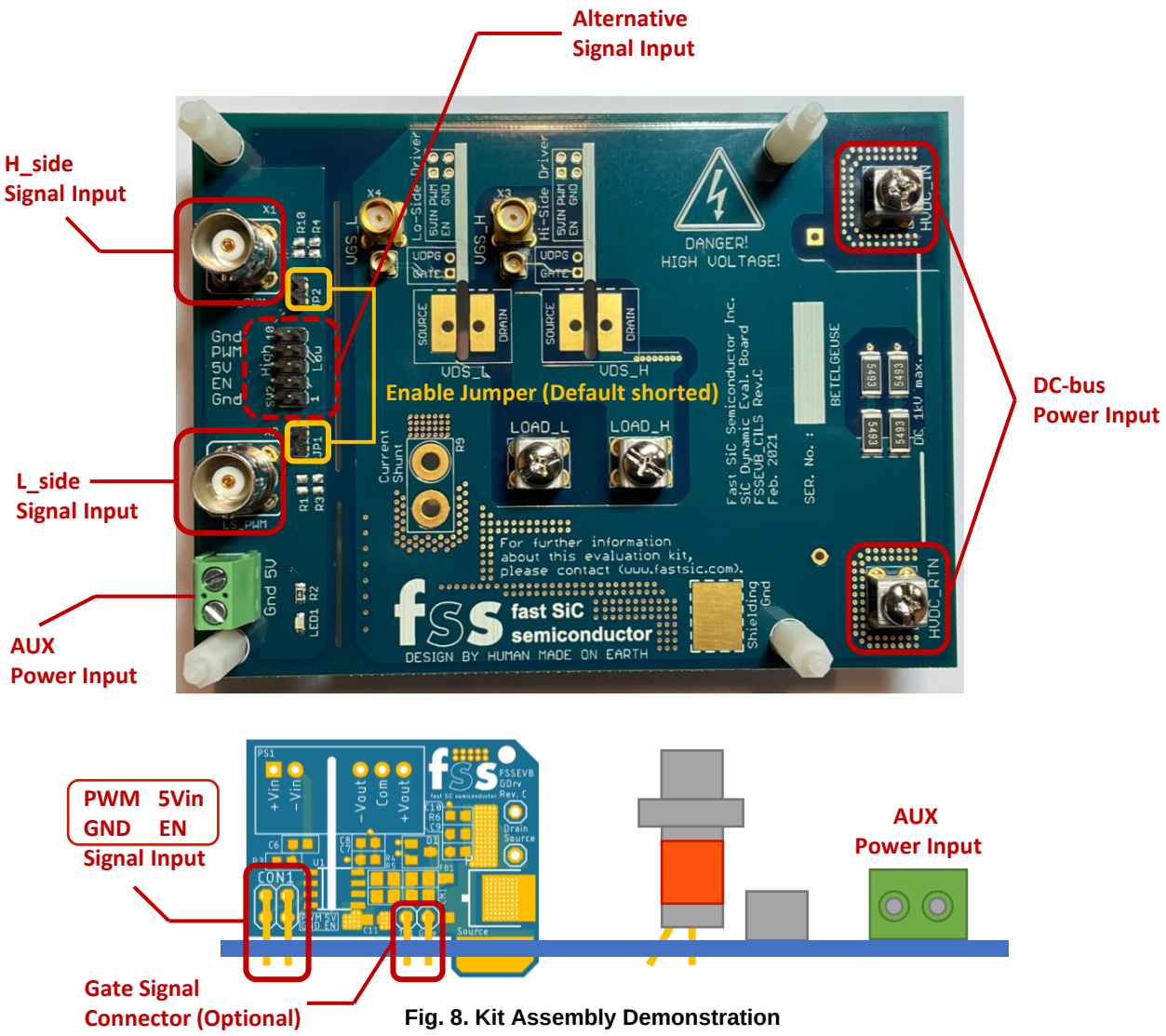

Fig. 8. Kit Assembly Demonstration

2.3.3 Signal Probing Instruction

A. Test Point Location:

For reducing the parasitic ringing phenomenon and improving the transient measurement accuracy, please shorten the ground loop on the probes if possible. For some specific probing tools (e.g. IsoVu kit from Tektronix, or others.), FSS also provides additional MMCX and SMA ports for the high common-mode noise immunity gate signal measurement. In order to implement these ports, please connect the gate voltage test point on the FSSEVB_GDrv board with the related ports on the FSSEVB_CILS kit, as Fig. 9 shown.

The critical signal probing test points on the FSSEVB_CILS evaluation kit and FSSEVB_GDrv daughter board are shown below:

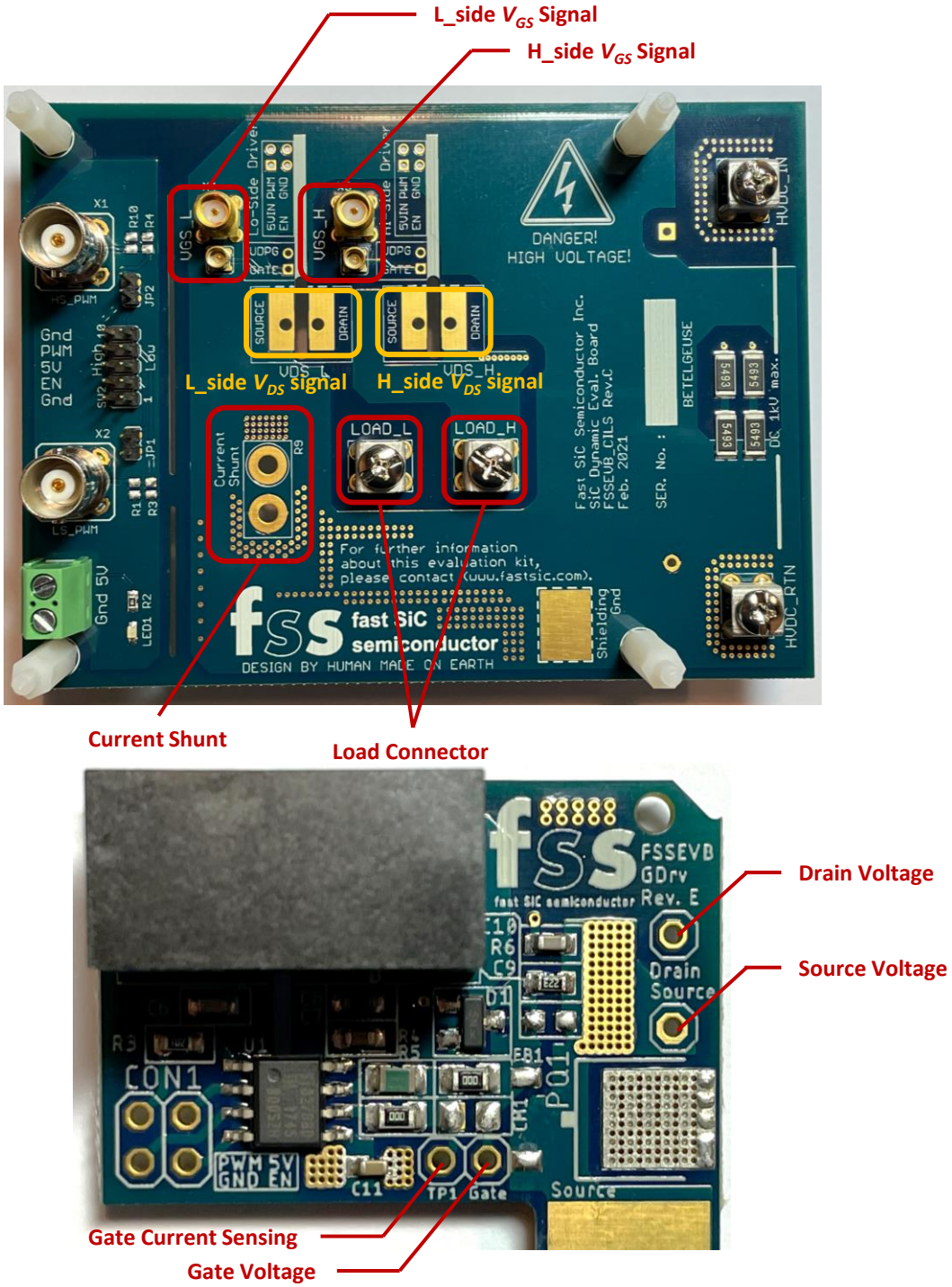

Fig. 9. Significant Test Points on Evaluation Kit

B. Probing Method Instructions:

To evaluate the high speed and wide range transient waveform, please carefully follow the instruction below.

- When measuring V_{DS} and V_{GS} , the measurement setup must have minimal loop between signal and ground. BNC, SMA, and MMCX connections can perform the best signal fidelity. Fig. 10 and Fig. 11 show the difference in CH.1, the V_{GS} waveform, to demonstrate the difference between two kinds of measurement setups.
- In Fig. 10, when using a general 6 inches crocodile clip as a grounding connection, we can observe there are significant ringing phenomenon occurred at V_{GS} waveform. (see CH.1) This is due to the oscillation of the inductance in the ground loop. The false ringing phenomenon may cause the user to incorrectly evaluate the real behavior of the target waveform and cause some unpredictable failure in their system.
- In Fig. 11, the improved measurement method is implemented, which also could realize by BNC, SMA, or MMCX port for further better performance. When using a low-inductance grounding connection kit, compared to a general 6 inches crocodile clip, the CH.1 measured result is significantly improved and presented a clean waveform. This may help users to judge the realistic event and optimize the related circuit parameters to the best condition.
- Due to the propagation delay between voltage probes and current probes are typically different, the oscilloscope scope probes measuring V_{DS} and I_D must be de-skewed to align together.
- The bandwidth of the measurement equipment is also a critical condition to judge the signal fidelity. With some high slew rate events, the limited bandwidth will distort the waveform seriously. (see Fig. 12) In general, a recommended bandwidth for SiC MOSFET transient behavior measurement is at least 350MHz.

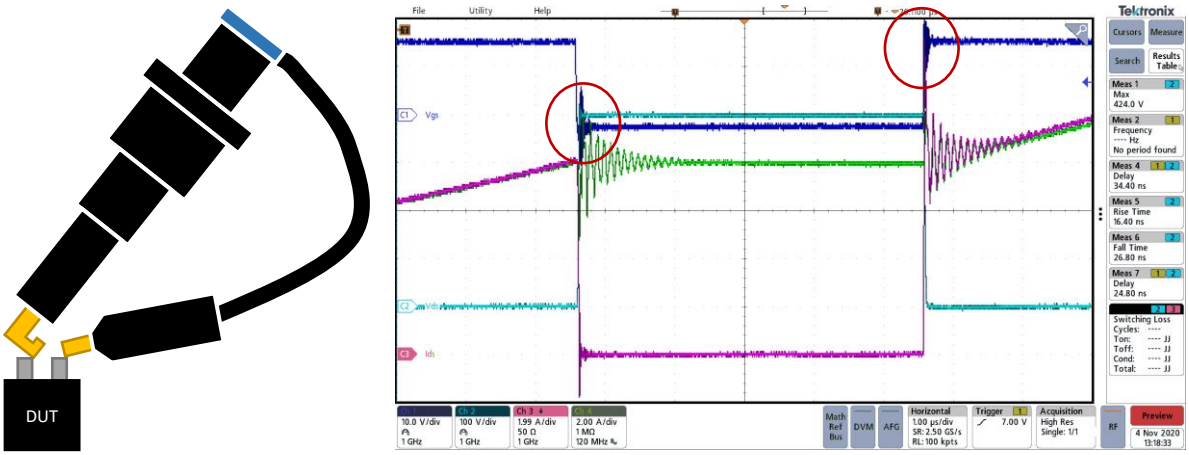

Fig. 10. Probing with a General 6 Inches Crocodile Clip as a Grounding Condition

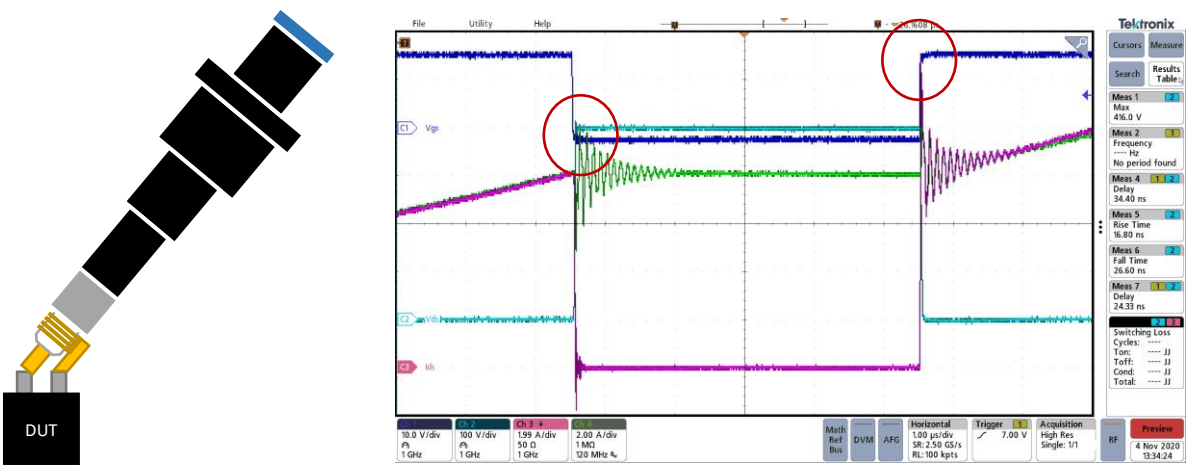

Fig. 11. Probing with a Low-inductance Ground Loop Connection Kit

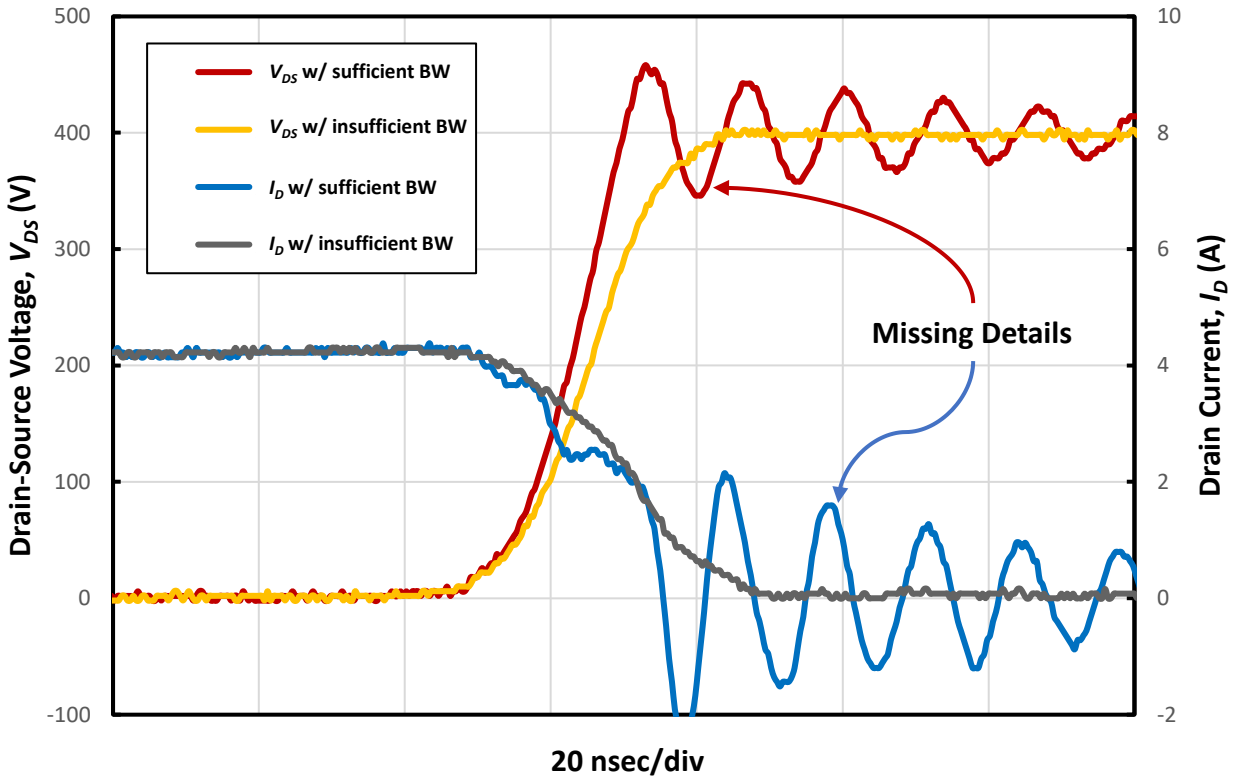

Fig. 12. A Typical Example of the Distortion Caused by Bandwidth Insufficient

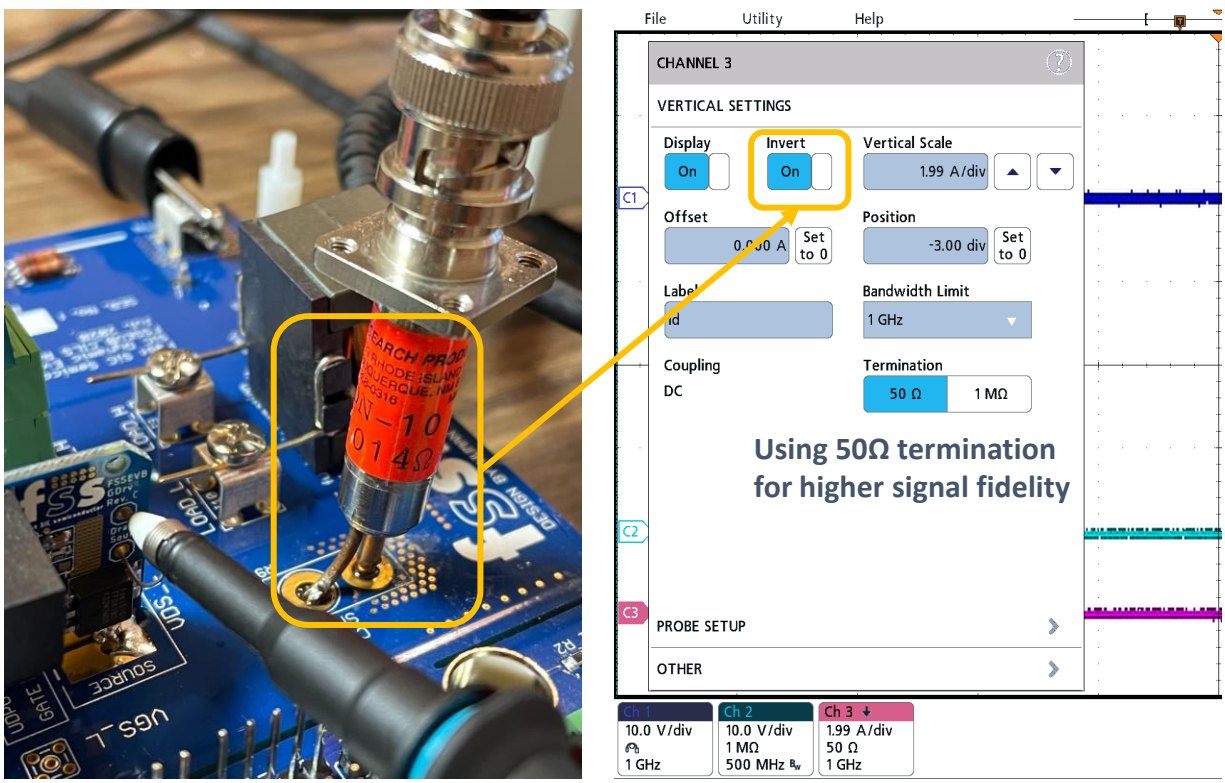

Fig. 13. Setup Example for Coaxial Shunt Resistor

2.4 Quick Start Guide

To evaluate Fast SiC Semiconductor Inc. SiC MOSFET, please follow the following instruction step-by-steps:

- Step 0. Assembly the FSSEVB_GDrv board on the related position on the FSSEVB_CILS board.

- Step 1. Populate the auxiliary power. For detail:
  - Connect the auxiliary power connector to apply a DC 5V for V_{AUX}. The auxiliary power could also be delivered directly by the DuPont terminals.

- Step 2. Drive-in related control signals in. For detail:
  - Drive in the related gate control signals with the BNC connectors or the DuPont terminals. Please noticed that in normal situation, the high side and low side gate signal should not be overlapped. In other words, the simultaneous "*high*" signal on both high side and low side gate signal are unacceptable. Therefore, if the user needs to push this command into the evaluation board, the users should clearly know what situation they'll face to and FSS will take NO responsibility under this operation.
  - Enable the EN pins by a logic high signal. In this case, the user can directly connect the EN pin to the auxiliary power by the jumper to active the gate driver at an always-on condition. Otherwise, the user could also control the enable signal by herself/himself.

- Step 3. Monitor the V_{GS} waveforms. For detail:
  - Monitor the V_{GS} waveforms to make sure the gate timing is as users expect/requirement.
  - Use an MMCX probe as the best solution, or a low capacitance SMA/BNC cable to reduce the rise and fall times and reject the unexpected noise.
  - Use a scope probe with a short ground loop soldered to the outside of the MMCX/SMA/BNC connector is also acceptable.

- Step 4. Populate the shunt resistor on R9 for current sensing requirements.
  - A high bandwidth shunt resistor is preferred, highly recommended to use SDN-10, a coaxial shunt resistor with 2GHz of bandwidth and noise rejected BNC terminal from T&M Research.

- Step 5. Populate the required load between H_Load and L_Load terminals.
  - Typically, a power resistor or a power inductor is a usual load option. When the clamped inductive load test (also known as "Double Pulse Test") is established, please noticed that a free-wheeling diode should be placed on high side to suppress the energy storage in the load inductor to avoid the D.U.T. be driven into avalanche mode.

- Step 6. Populate the DC-bus power to the target voltage level.

- Step 7. Monitor the V_{DS} waveforms. For detail:
  - Monitor the V_{DS} voltage using the test points on the FSSEVB_GDrv board with a short ground loop connection on an oscilloscope probe. Direct probing the V_{DS} voltage signal on the FSSEVB_CILS board is also acceptable, but for evaluating the accurate situation of the SiC MOSFET, the signal on the FSSEVB_GDrv board is more reliable.

- Step 8. Monitor the I_D waveforms. The preferred measurement method is to reverse-connect the shunt resistor as Fig. 13, then inverting the caught signal on the oscilloscope.

- Step 9. After finished the test, shut down the DC-bus power and waiting for the bleeding resistors to dissipate the redundant energy to a safe voltage level.

3. Applications

3.1 Example Topologies

This evaluation kit could do various behavior demonstration by changing the related connection of the different input/ output terminals and herein are some examples for reference:

3.1.1 Clamped Inductive Load Switching

A. Overview:

Clamped inductive load switching (CILS) is a well-known test method to evaluate the dynamic parameters of a diode/transistor. CILS test can simply discover the switching time, switching energy, switching charge, diode reverse recovery characteristics, dv/dt ruggedness, and other transient behaviors with simultaneously delivering a high V_{DS} and high I_D into a D.U.T. The schematic is shown in Fig. 15.

B. Operating Principle:

To evaluate the dynamic behavior of the D.U.T., simultaneously given a rated V_{DS} and I_D on a switching platform, eliminate the influence of other components is necessary. CILS test is a simple way to complete this mission. With a typical half-bridge topology, a power inductor is placed on the top side in parallel. The theoretical waveform and procedure are shown in Fig. 16.

First, in $t_1 - t_2$, a double pulse (or multi-pulse) signal is delivered to the D.U.T. at the bottom side. The first pulse could decide the target testing current in this experiment by charging the inductor. The pulse-width of the first pulse and the DC-bus voltage could determine the rated current by eq.1, please note that the current can not exceed the saturation current of the related power inductor.

$$V_{DC} = L\frac{di}{dt} \quad (1)$$

In $t_2 - t_3$, after charging the inductance current to the target spec., turning off the D.U.T. Meanwhile, the inductor requires a continuous current commutation path to release magnetic energy. Thus, the inductance current will force the body diode to on-state as a free-wheeling diode. And the current is stored in this loop. Please notice that without the free-wheeling diode, the test will transfer to unclamped inductive load switching, which will induce a tremendous high voltage and push the D.U.T. to the avalanche mode. This will be harmful and extremely dangerous.

Finally, in $t_3 - t_6$, turning on the D.U.T. again, the current stored in the inductor loop will immediately pass thru the D.U.T., which means the user could observe the switching behavior of the D.U.T. within a simultaneously high-voltage and high-current condition. In this test, $t_3 - t_4$ is the turn on transition and $t_5 - t_6$ is the turn off transition.

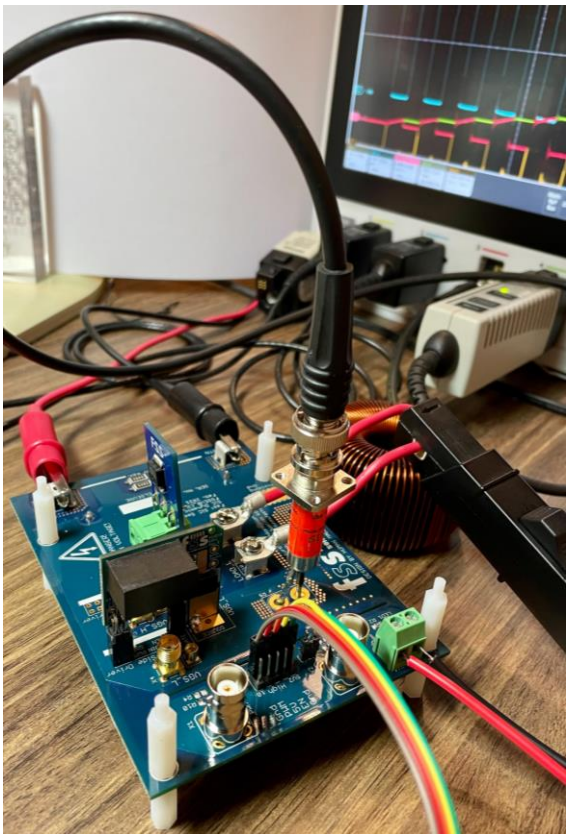

Fig. 14. Practical Setup – Clamped Inductive Load Switching

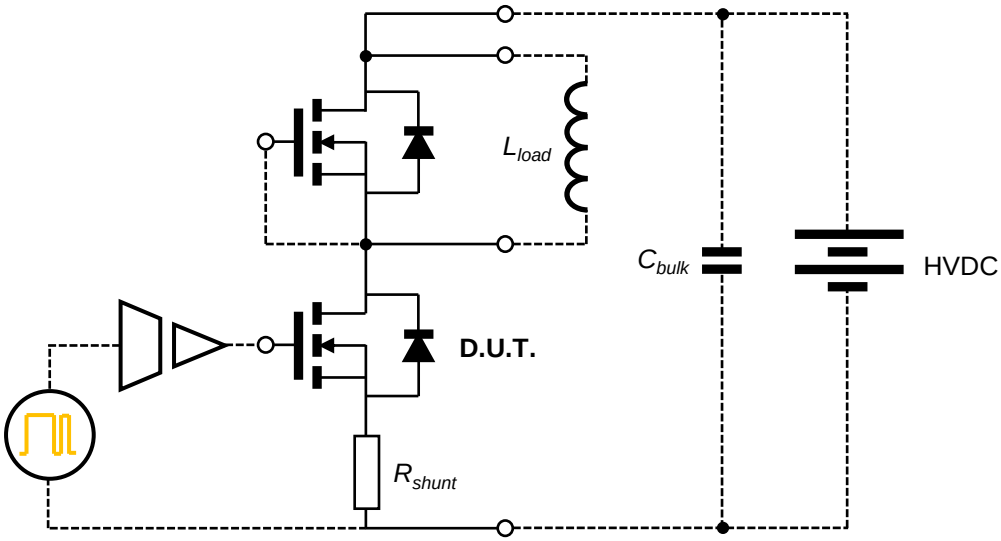

Fig. 15. Example Topologies – Clamped Inductive Load Switching

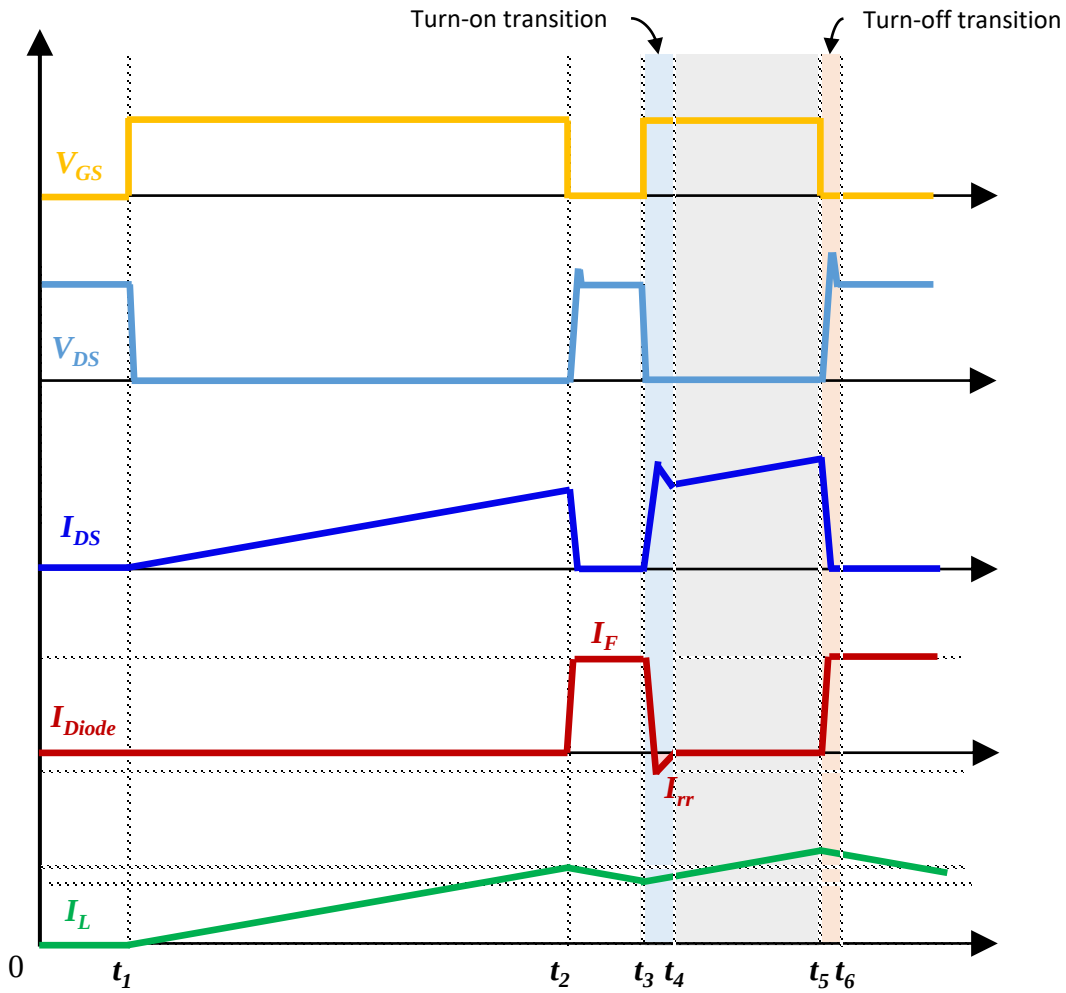

Fig. 16. Theoretical Waveform – Clamped Inductive Load Switching

3.1.2 Resistive Load Switching

A. Overview:

Resistive load switching is another test method to evaluate the dynamic parameters of a transistor. Resistive load switching test can simply discover the switching time, switching energy, switching charge, dv/dt ruggedness, and other transient behaviors with simultaneously delivering a rated V_{DS} and rated I_D into a D.U.T. The schematic is shown in Fig. 17.

B. Operating Principle:

The operating principle of resistive switching is simpler than a CILS test. A power resistor should be applied in this test as a current limiter. The switching current always follows the Ohmic law as eq. 2.

In this test, a non-inductive resistor is preferred to reduce the overshoot in turn off transient.

$$V_{DC} = \left(R_{D.U.T.} + R_{Load} + R_{stray}\right) \times I \quad (2)$$

Since the trajectory of operation points of resistive switching and inductive switching are different (see Fig. 18), users could reference these two test results to evaluate their switching behavior in a specific application.

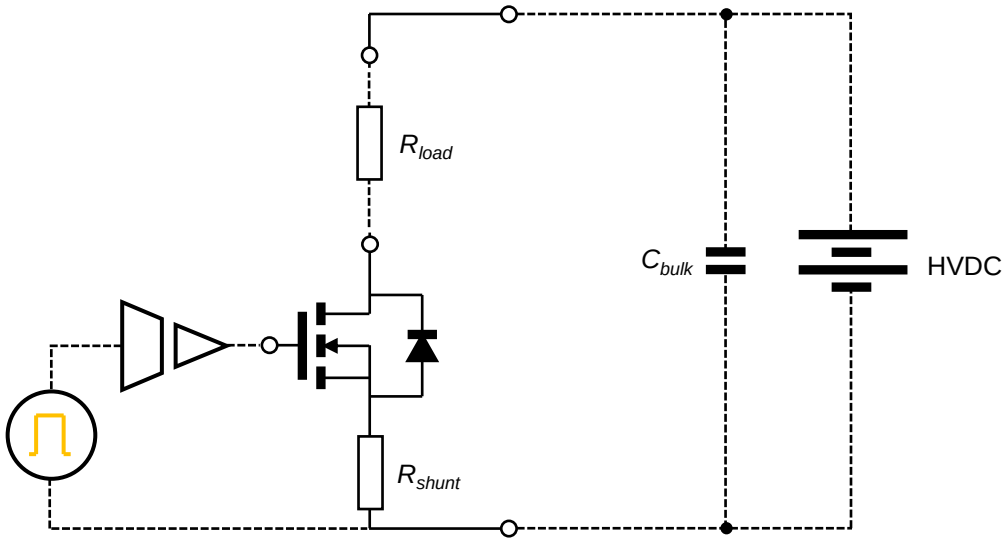

Fig. 17. Example Topologies – Resistive Load Switching

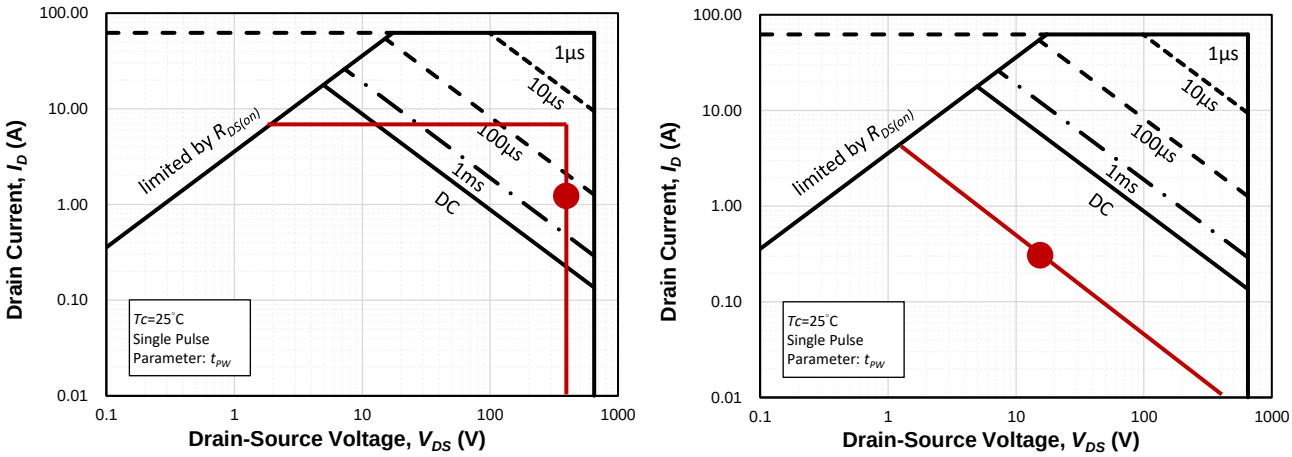

Fig. 18. An Example of Trajectory of Operation Points (Left: Clamped Inductive Load ; Right: Resistive Load)

3.2 Ideal and Practical Switching Waveform of SiC MOSFET

3.2.1 Ideal Switching Waveforms (Inductive Load)

In general, the ideal switching waveforms of a SiC MOSFET could be demonstrated as Fig. 19. The detailed trajectories of the following statement are listed in the following table. Noted that the C_{iss_1} in each equations is a function of voltage from the rated V_{DS} value to V_{DS}=0, then continuing with V_{GS}=0 to V_{Miller}; the C_{iss_2} in each equations is a function of voltage from V_{Miller} to V_{GS_on}.

Theoretical Waveform Description – Ideal Inductive Switching

Stage	Description
Turn-on delay (t_1 -> t_2)	$t_{delay,on} = R_G \cdot C_{iss\_1} \cdot ln\left(\frac{V_{GS\_on}}{V_{GS\_on} - V_{th}}\right)$
Current rising (t_2 -> t_3)	$t_{current,r} = R_G \cdot C_{iss\_1} \cdot ln\left(\frac{V_{GS\_on} - V_{th}}{V_{GS\_on} - V_{Miller}}\right)$
Voltage falling (Miller plateau) (t_3 -> t_4)	$t_{volt,f} = \frac{Q_{GD} \cdot R_G}{V_{GS\_on} - V_{Miller}}$
Gate Rising (t_4 -> t_5)	$t_{gate,r} = R_G \cdot C_{iss\_2} \cdot ln\left(\frac{V_{GS\_on}}{V_{GS\_on} - V_{Miller}}\right)$
Turn-off delay (t_6 -> t_7)	$t_{gate,f} = R_G \cdot C_{iss\_2} \cdot ln\left(\frac{V_{GS\_on}}{V_{Miller}}\right)$
Voltage Rising (Miller plateau) (t_7 -> t_8)	$t_{volt,r} = \frac{Q_{GD} \cdot R_G}{V_{Miller}}$
Current falling (t_8 -> t_9)	$t_{current,f} = R_G \cdot C_{iss\_1} \cdot ln\left(\frac{V_{Miller}}{V_{th}}\right)$
Gate falling (t_9 -> t_{10})	V_{gate} continues to drop to zero (C_{GS} be totally discharged)

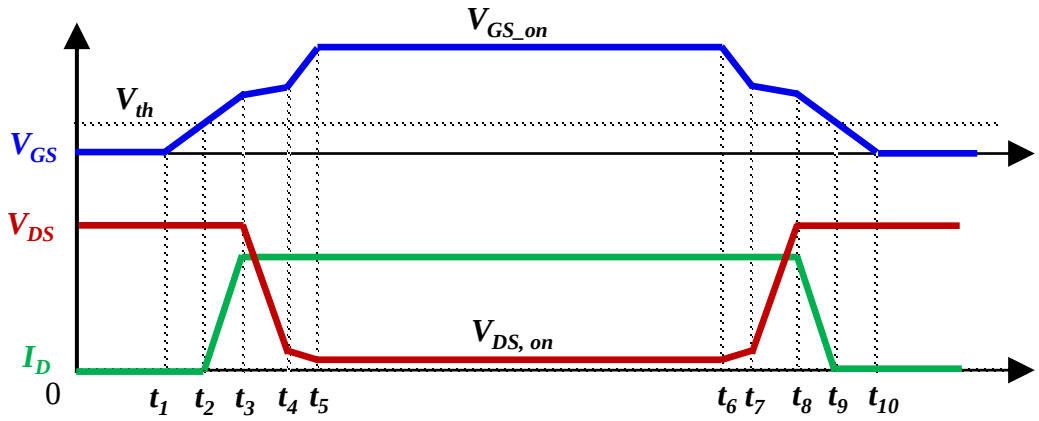

Fig. 19. Ideal Waveform –Inductive Load Switching

3.2.2 Practical Switching Waveforms (Inductive Load)

Coming to the dynamic behavior, an ideal switch has approximated zero rise time and fall time, thus the switching loss is zero and the transition waveforms are clear. However, the switching behavior is actually a rather complex association of several parasitic components, which have significant influence on the practical switching event. Since the switching velocity of wide band-gap devices are more rapid than conventional silicon devices, the transient behavior of the wide band-gap devices is far more sensitive to parasitic components. Fig.20 and Fig. 21 shows a typical switching waveform of a SiC MOSFET. In this case, some general behaviors are explained as following:

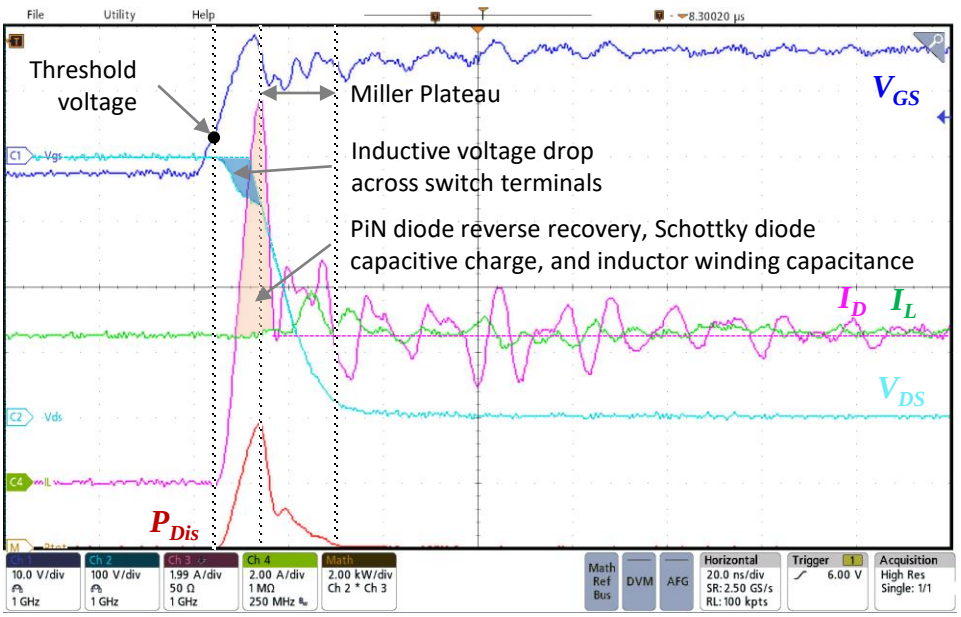

Fig. 20. Practical Turn-on Waveform – Clamped Inductive Load Switching

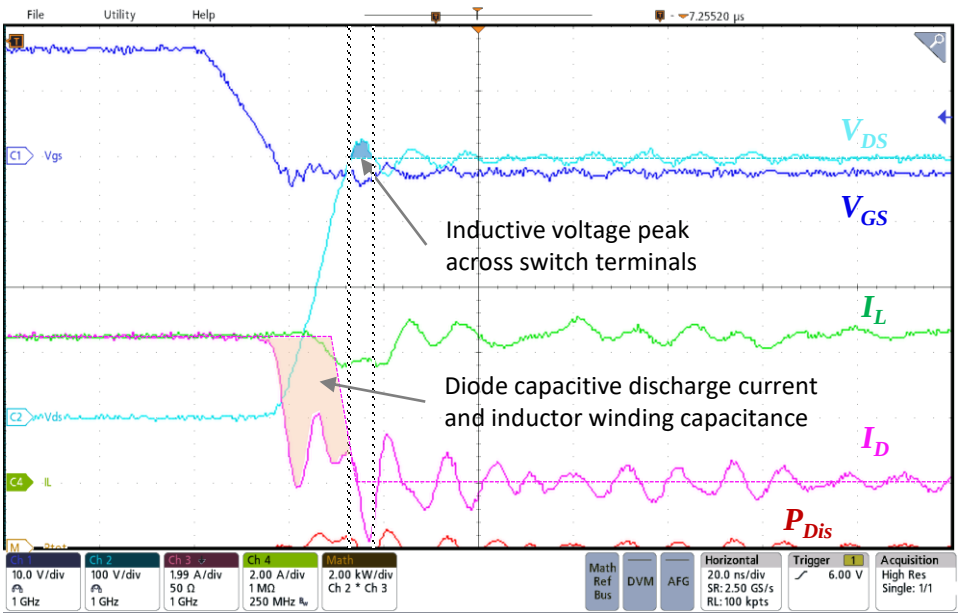

Fig. 21. Practical Turn-off Waveform – Clamped Inductive Load Switching

3.3 Process Chart for Selecting a SiC MOSFET

The following flow chart is a simple selection procedure of SiC power MOSFET for the target system spec. To earn further information, the user could contact specialists in Fast SiC semiconductor Inc.

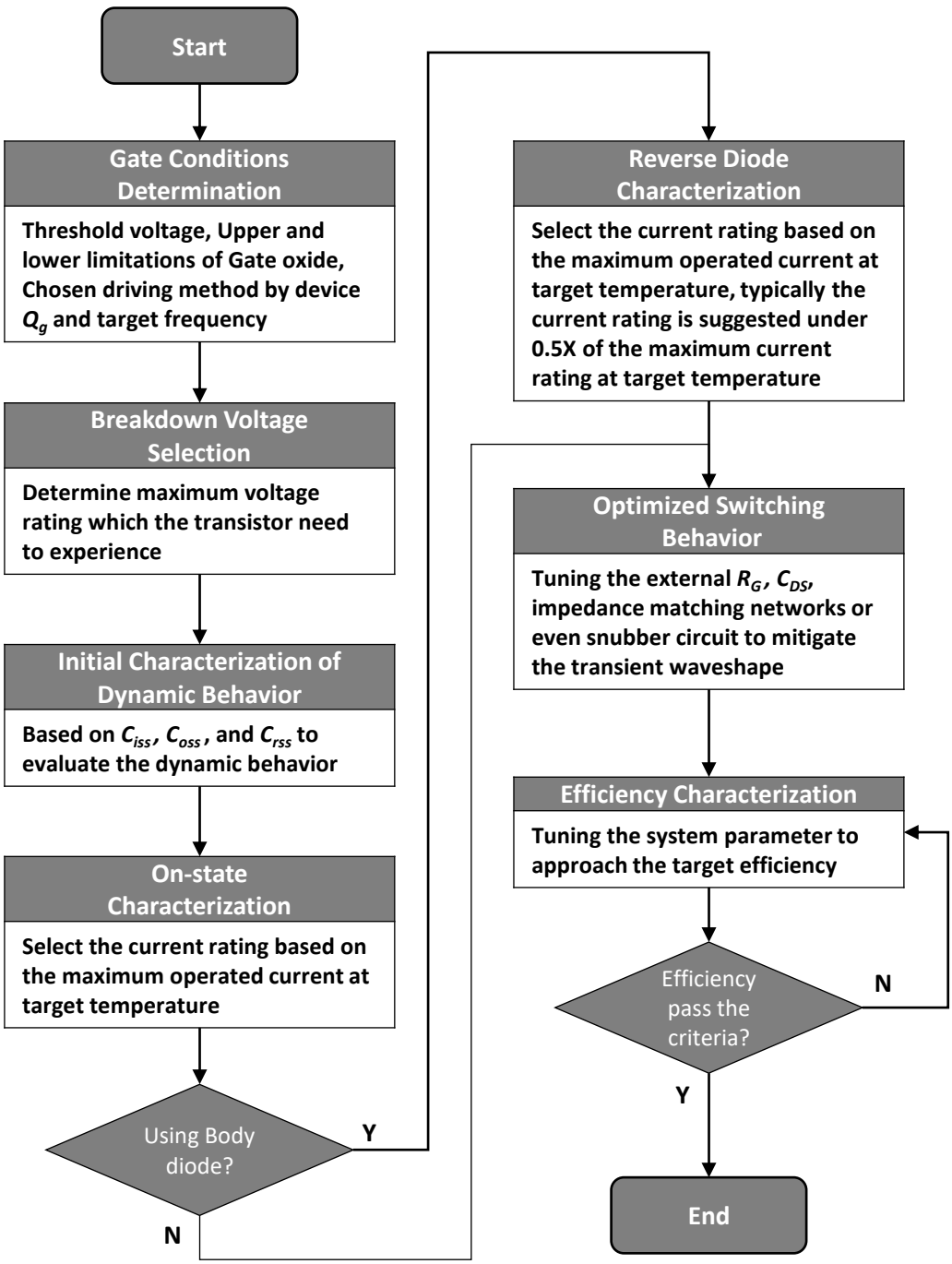

Fig. 22. Process Flow Chart for Selecting a SiC MOSFET

4. Manufacturing Information

4.1 Schematic

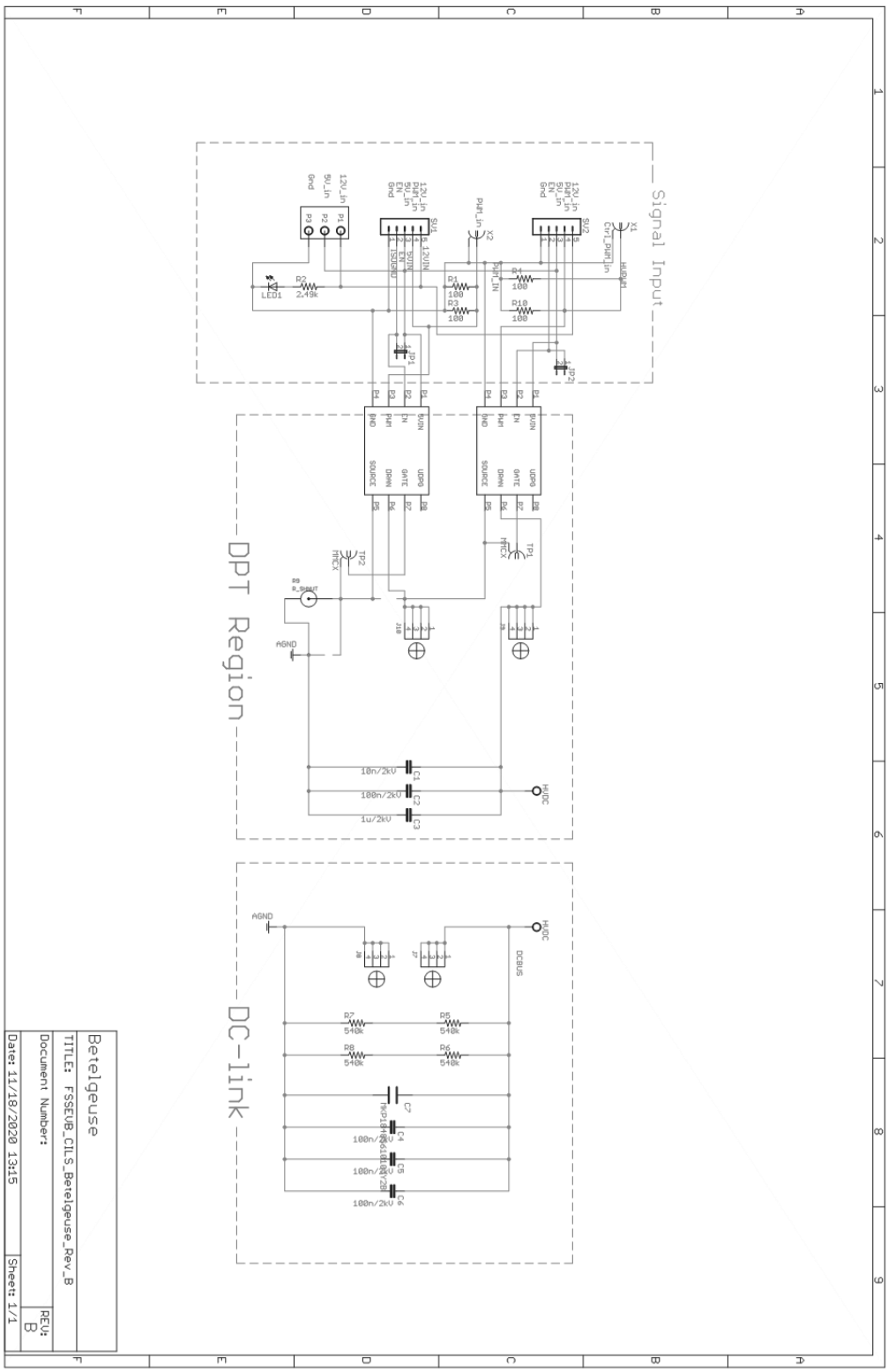

Fig. 23. Schematic of FSSEVB_CILS

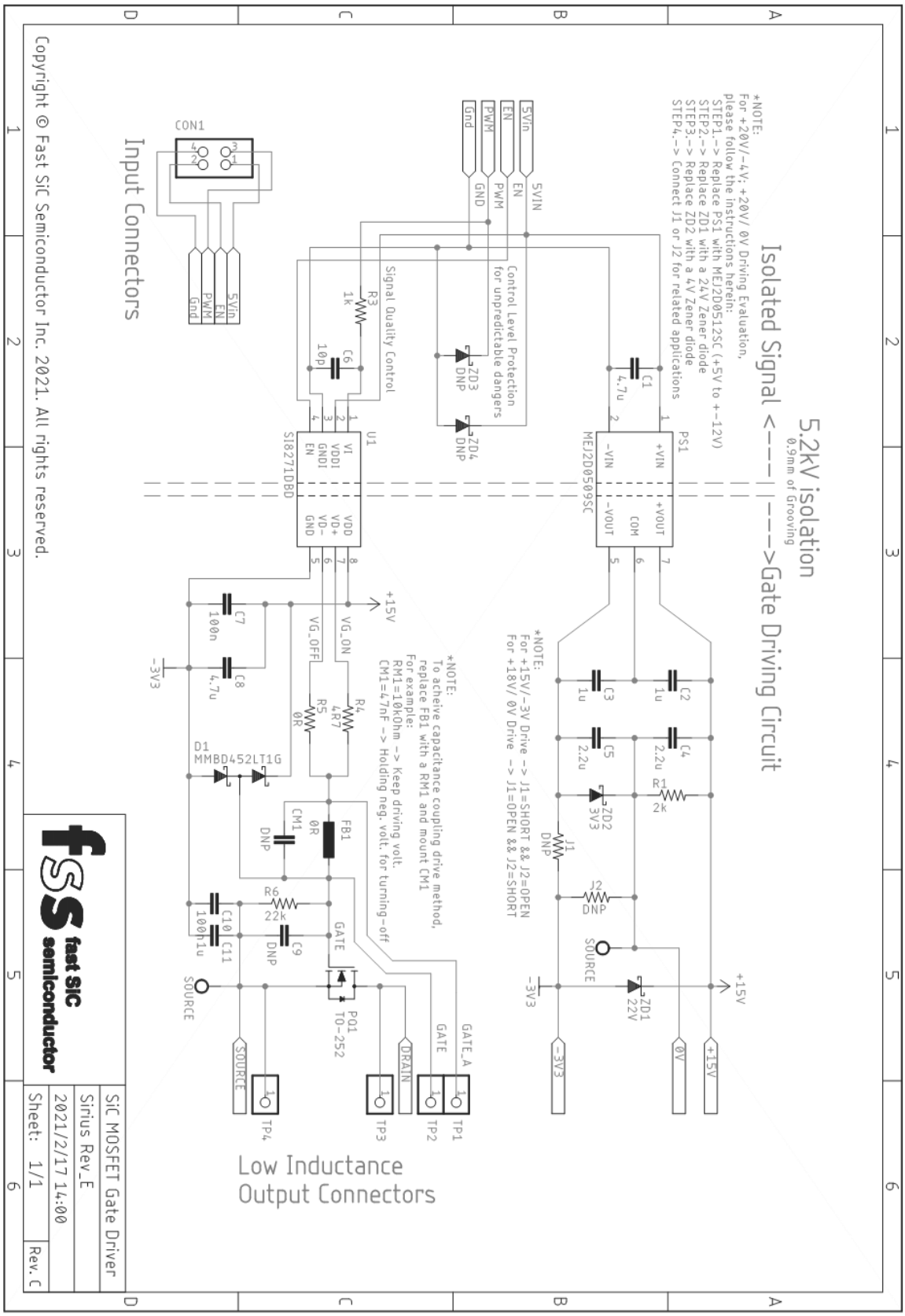

Fig. 24. Schematic of FSSEVB_GDrv

4.2 PCB Layout

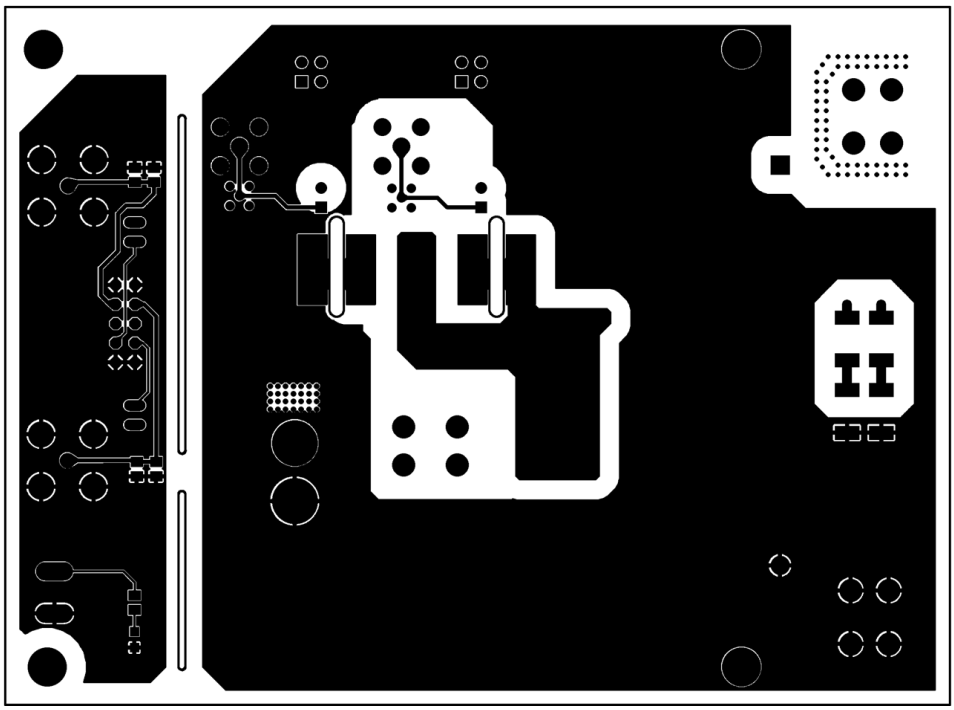

Fig. 25. Top Layer of FSSEVB_CILS

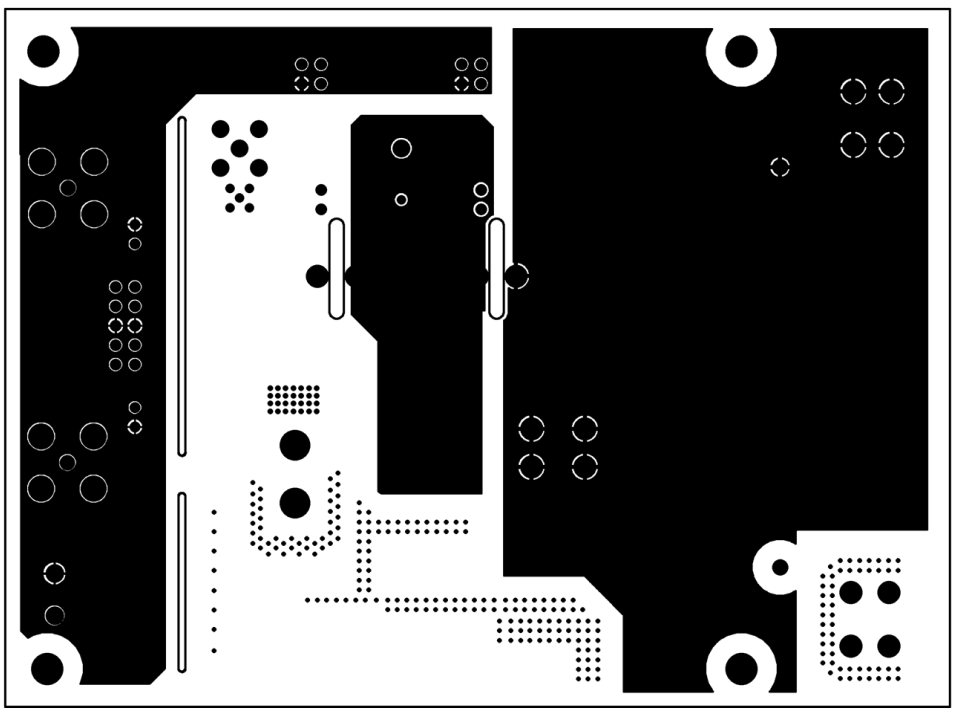

Fig. 26. 2nd Layer of FSSEVB_CILS

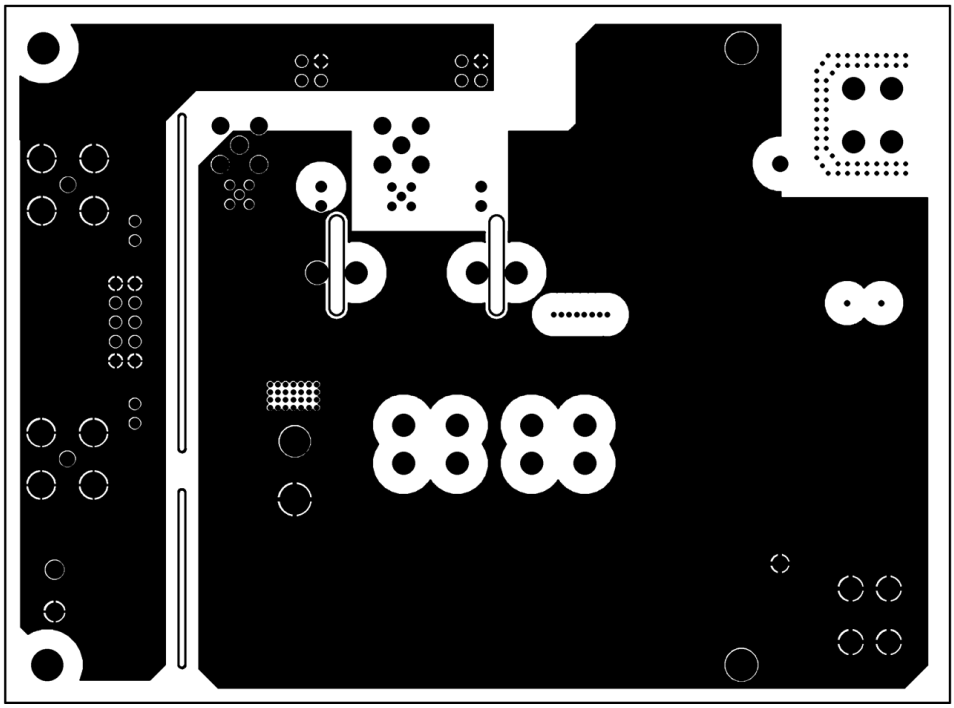

Fig. 27. 3rd Layer of FSSEVB_CILS

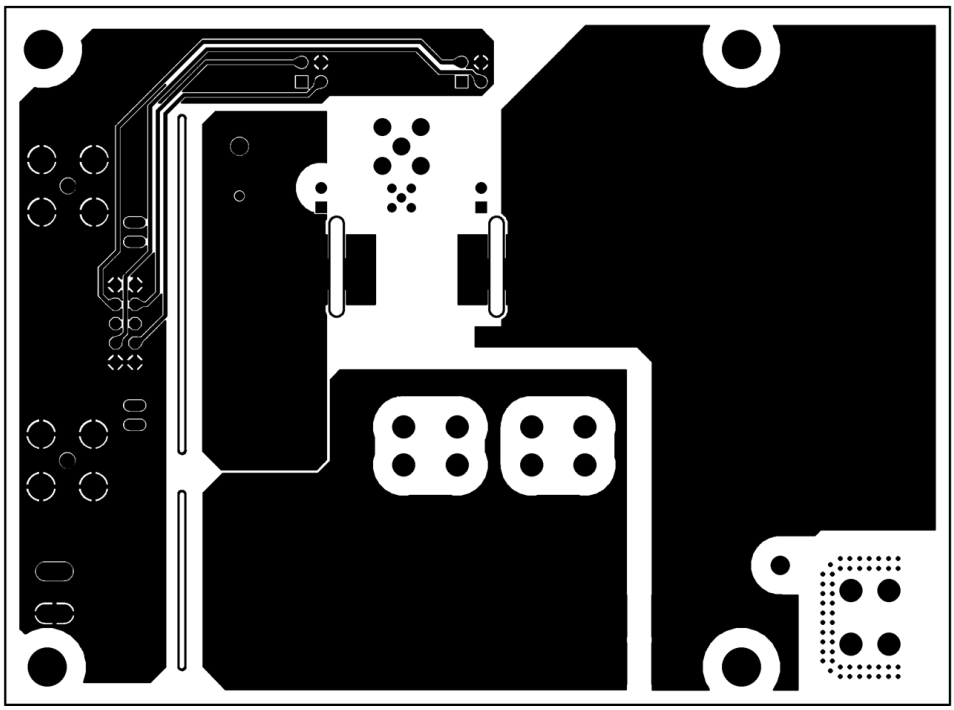

Fig. 28. Bottom Layer of FSSEVB_CILS

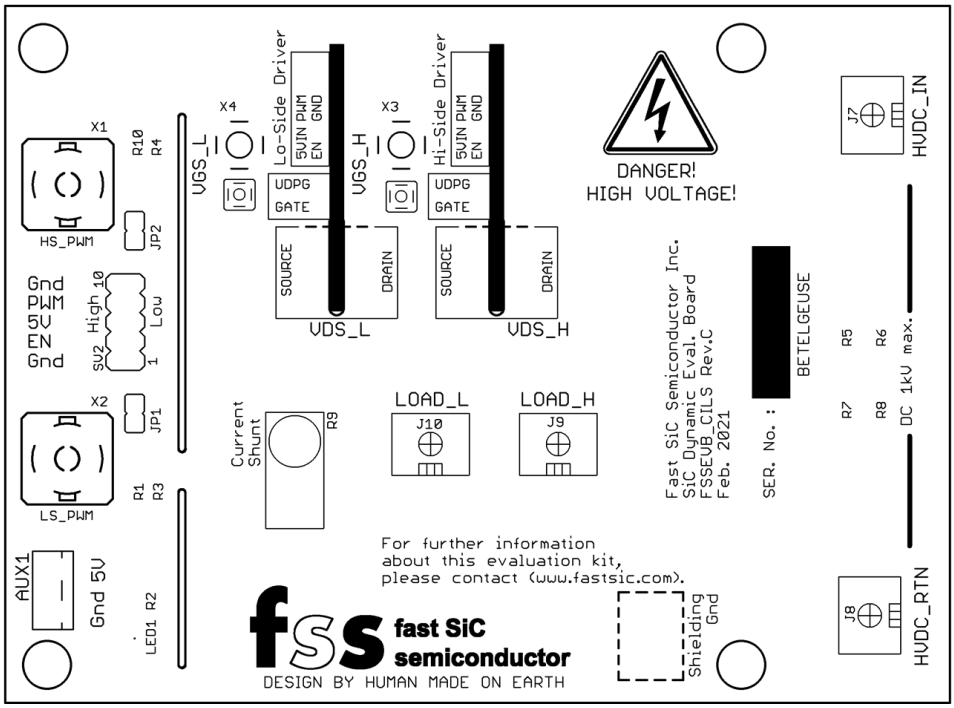

Fig. 29. TOP Silkscreen of FSSEVB_CILS

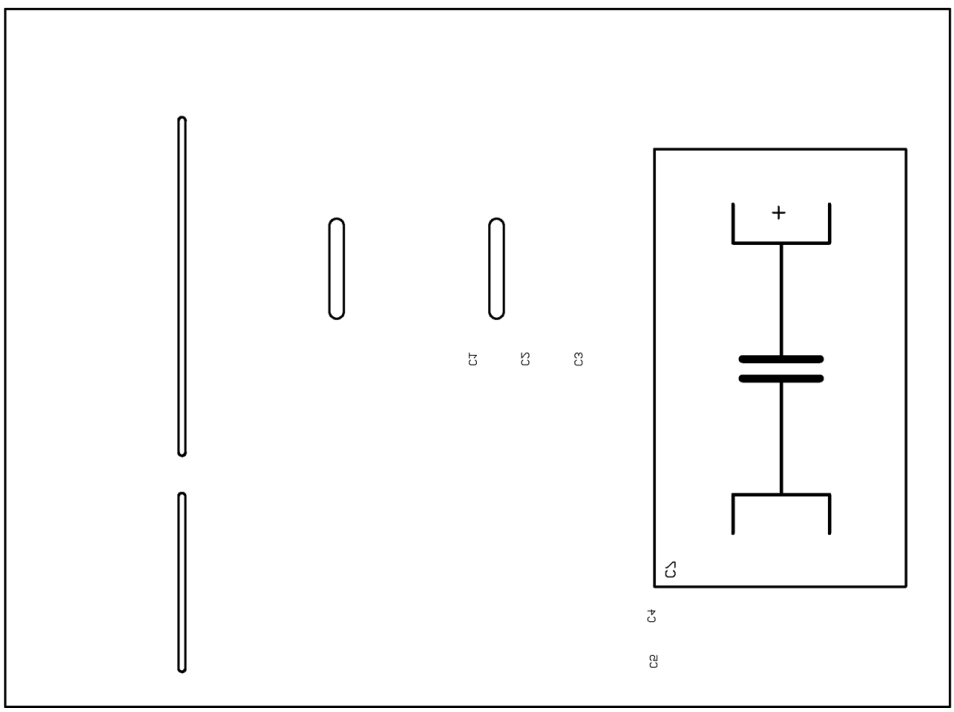

Fig. 30. Bottom Silkscreen of FSSEVB_CILS

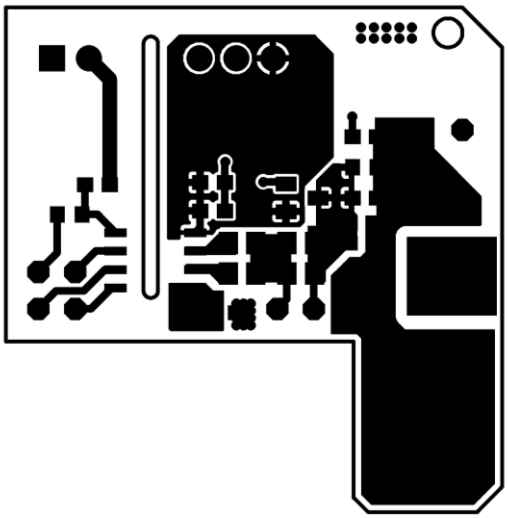

Fig. 31. Top Layer of FSSEVB_GDrv

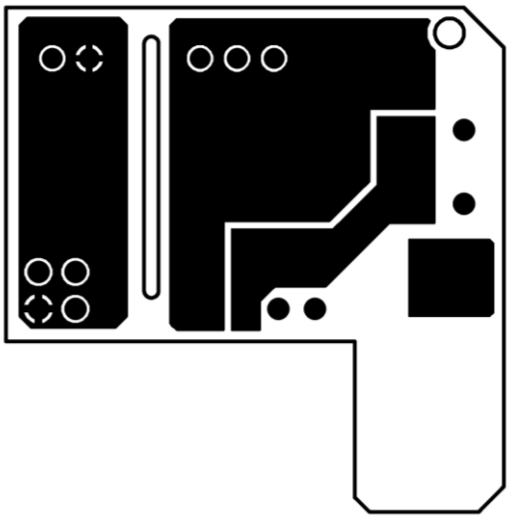

Fig. 32. 2nd Layer of FSSEVB_GDrv

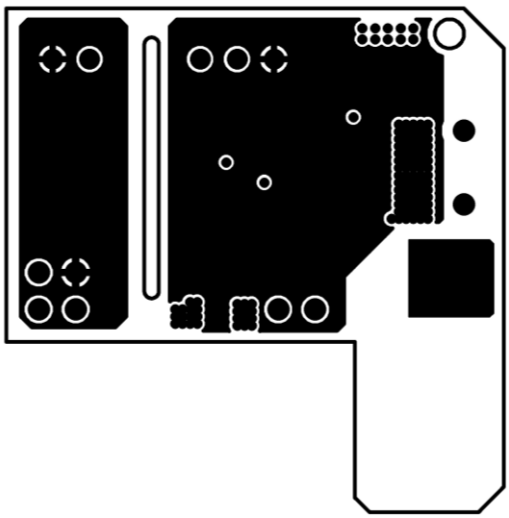

Fig. 33. 3rd Layer of FSSEVB_GDrv

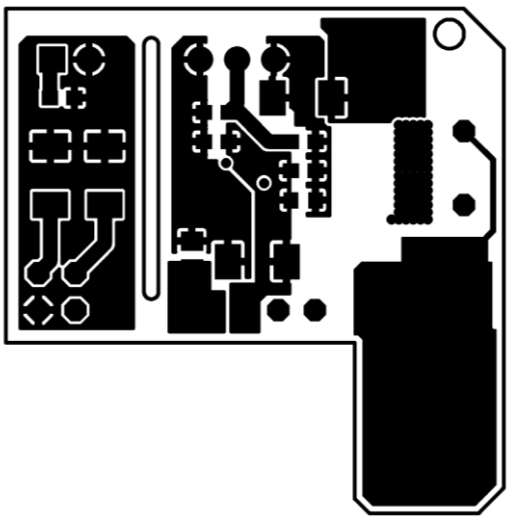

Fig. 34. Bottom Layer of FSSEVB_GDrv

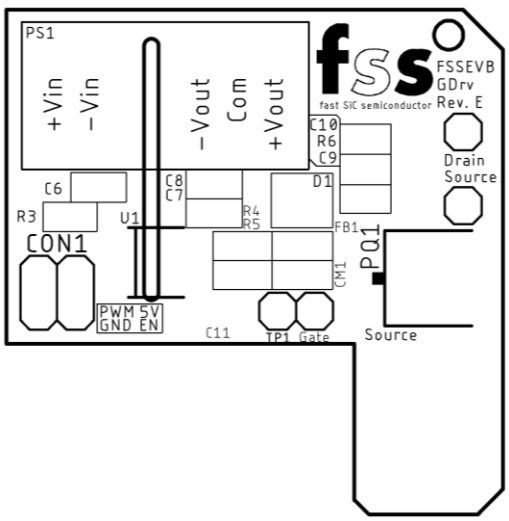

Fig. 35. TOP Silkscreen of FSSEVB_GDrv

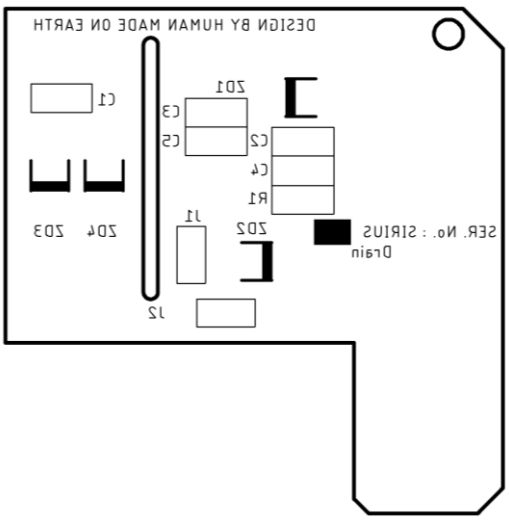

Fig. 36. Bottom Silkscreen of FSSEVB_GDrv

4.3 Bill of Materials

B.O.M.				
Part	**Value**	**Part number**	**Brand**	**Description**
Gate Driving Daughter Board				
C1, C8	4.7u	GRT188R6YA475KE13D	Murata	CAP CER 4.7UF 35V X5R 0603
C2, C3, C11	1u	GRT188R61H105KE13D	Murata	CAP CER 1UF 50V X5R 0603
C4, C5	2.2u	GRT188R61H225KE13D	Murata	CAP CER 2.2UF 50V X5R 0603
C6	10p	GCM1885C2A100JA16D	Murata	CAP CER 10PF 100V C0G/NP0 0603
C7, C10	100n	GCJ188R71H104KA12D	Murata	CAP CER 0.1UF 50V X7R 0603
C9	DNP	--	--	--
CM1	DNP	--	--	--
CON1	--	--	--	--
D1	30V	MMBD452LT1G	ON Semiconductor	SCH DIODE 30V 225mW SOT23-3
FB1	0R	ERJ-6GEY0R00V	Panasonic	RES SMD 0 OHM JUMPER 1/8W 0805
J1, J2	DNP	--	--	--
PQ1[(1)]	190m	FF06190A	fast SiC semiconductor	SiC MOSFET 650V 190mOHM TO-252
PS1	+-9V	MEJ2D0509SC	Murata	DC DC CONVERTER +/-9V 2W
R1	2k	ERJ-3EKF2001V	Panasonic	RES 2K OHM 1% 1/10W 0603
R3	1k	ERJ-3GEYJ102V	Panasonic	RES 1K OHM 5% 1/10W 0603
R4	5R9	PTN0805K5R90FST1	Vishay Thin Film	RES 5.9 OHM 0.1% 1/5W 0805
R5	0R	ERJ-6GEY0R00V	Panasonic	RES 0 OHM 1/8W 0805
R6	22k	ERA-3AED223V	Panasonic	RES 22K OHM 0.5% 1/10W 0603
U1	SI8271DBD	SI8271DBD-IS	Silicon Labs	4A 2.5 KV DRIVER SOIC-8
ZD1	22V	1SMA5933BT3G	ON Semiconductor	DIODE ZENER 22V 1.5W SMA
ZD2	3V3	1SMA5913BT3G	ON Semiconductor	DIODE ZENER 3.3V 1.5W SMA
ZD3, ZD4	6V	SZ1SMA5919BT3G	ON Semiconductor	DIODE ZENER 5.6V 1.5W SMA
Clamped Inductive Load Carrier				
AUX1	2L_JACK	VI0221520000G	Amphenol Anytek	TERM BLK 2P SIDE ENT 5.08MM PCB
C1	10n/2kV	GR455DR73D103KW01L	Murata	CAP CER 10000PF 2KV X7R 2220
C2, C4, C5, C6	100n/1kV	C2220C104KDRACAUTO	KEMET	CAP CER 2220 0.1UF 1000V X7R
C3	0.47u/1kV	2220Y1K00474KETWS2	Knowles Syfer	CAP CER 0.47UF 1KV X7R 2220
C7	10u/1kV	MKP1848S61010JY2B	Vishay Beyschlag	CAP FILM 10UF 5% 1KVDC RADIAL
J7, J8, J9, J10	15ADC	7691 (power socket)	Keystone Electronics	TERM SCREW 6-32 4 PIN PCB
JP1, JP2	2P	10129378-902003BLF	Amphenol ICC (FCI)	CONN HEADER VERT 2POS 2.54MM
LED1	GREEN	LG R971-KN-1	OSRAM	LED GREEN DIFFUSED 0805 SMD
R1, R3, R4, R10	DNP	--	--	--
R2	300	ERJ-6GEYJ301V	Panasonic	RES SMD 300 OHM 5% 1/8W 0805
R5, R6, R7, R8	549k	ERJ-1TNF5493U	Panasonic	RES SMD 549K OHM 1% 1W 2512
R9[(1)]	R_SHNUT	SDN-10	T&M Research	RES 0.1OHM 2000MHZ EMAX=2JULES
SV2	10P	10129381-910003BLF	Amphenol ICC (FCI)	CONN HEADER VERT 10POS 2.54MM
TP1, TP2	MMCX	0734151471	Molex	CONN MMCX JACK STR 50 OHM
X1, X2	BNC	112538	Amphenol	CONN BNC RCPT STR 50 OHM PCB
X3, X4	SMA	0733910070	Molex	CONN SMA RCPT STR 50 OHM PCB

[(1)] Not included in this kit.

5. Typical Performance Curves

5.1 Important Curves and Waveform

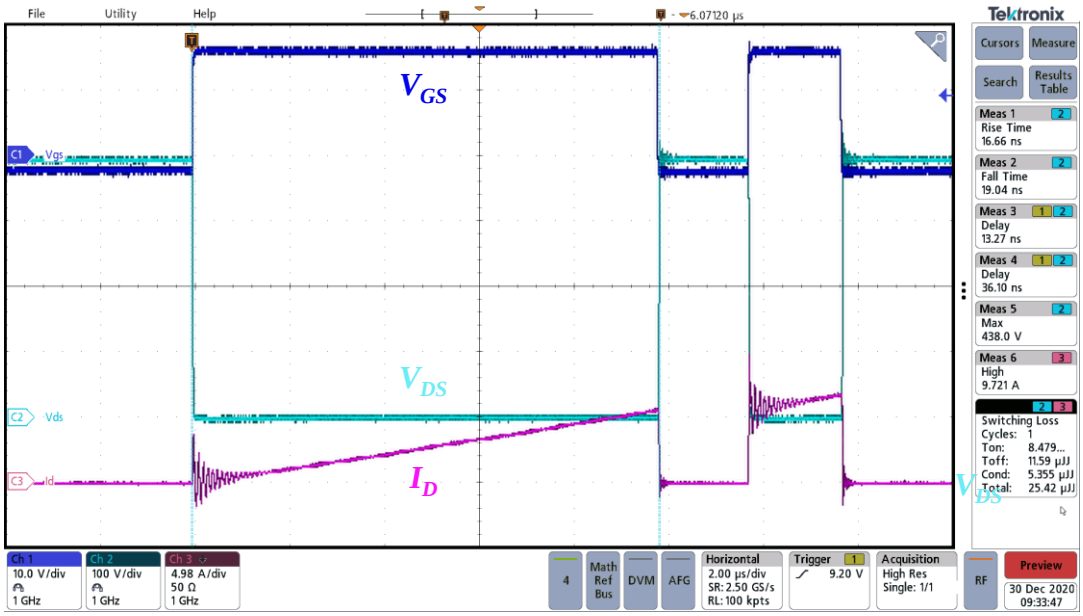

Fig. 37. Double Pulse Test with FF06190A and 670µH Inductor

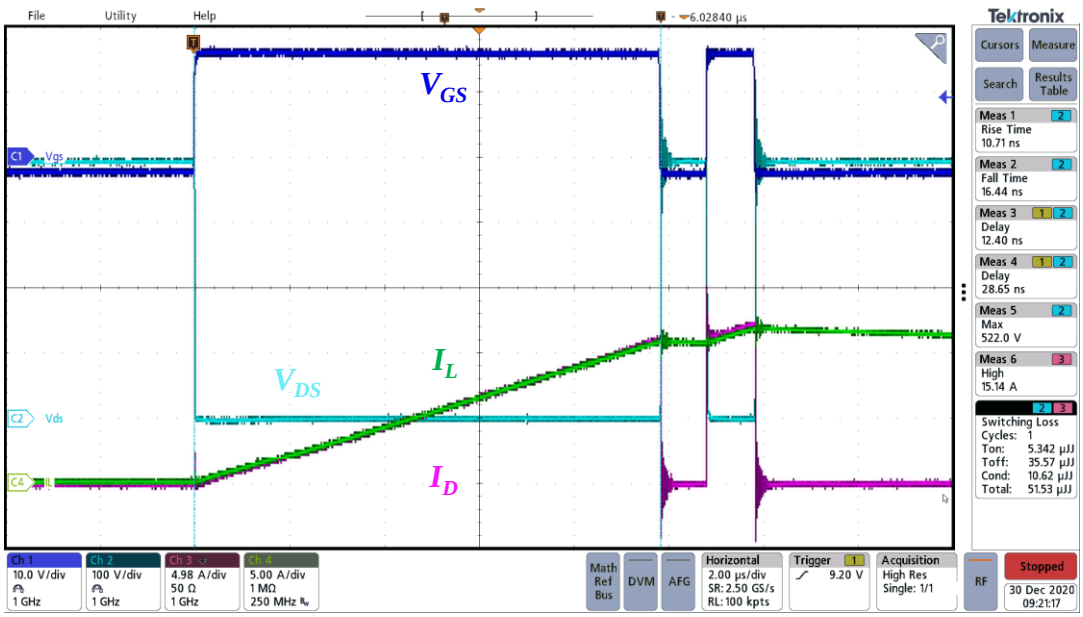

Fig. 38. Double Pulse Test with FF06190A and 340µH Inductor

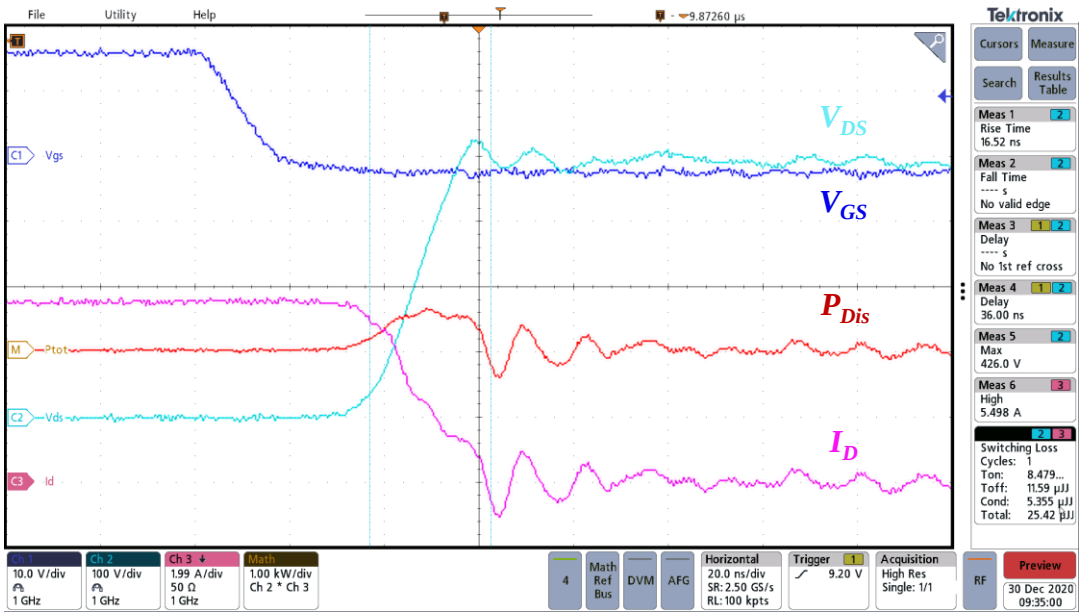

Fig. 39. Turn-off Transient of Double Pulse Test with FF06190A and 670µH Inductor

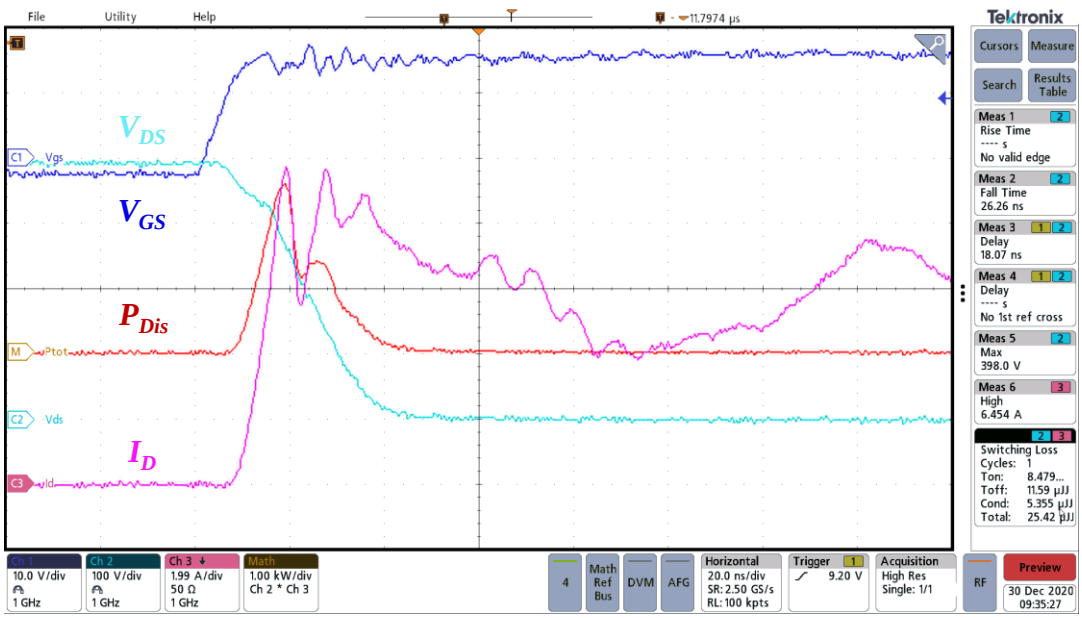

Fig. 40. Turn-on Transient of Double Pulse Test with FF06190A and 670µH Inductor

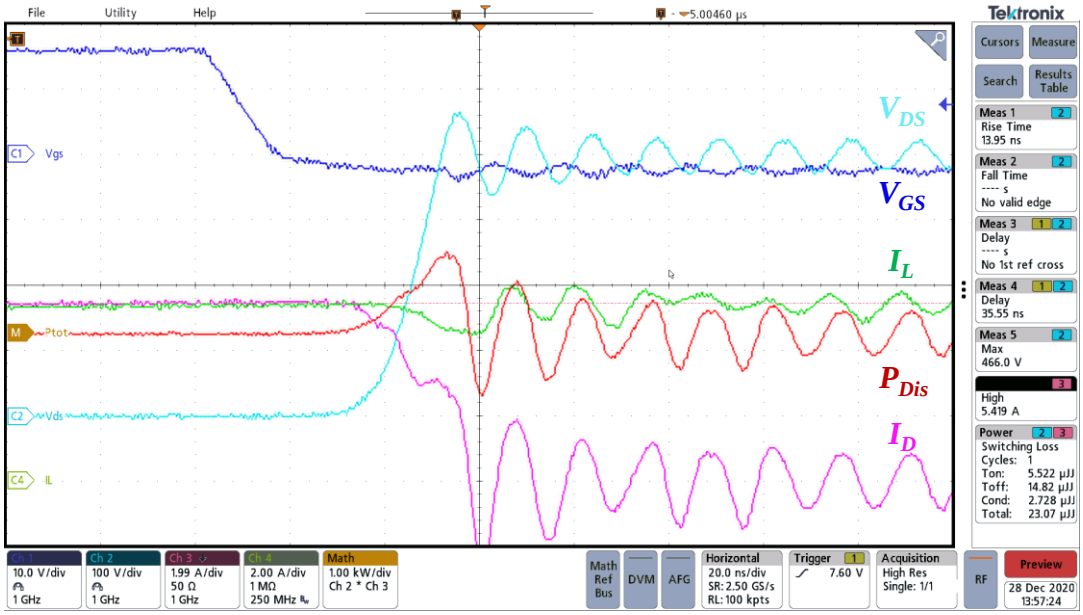

Fig. 41. Turn-off Transient of Double Pulse Test with FF06190A and 340µH Inductor

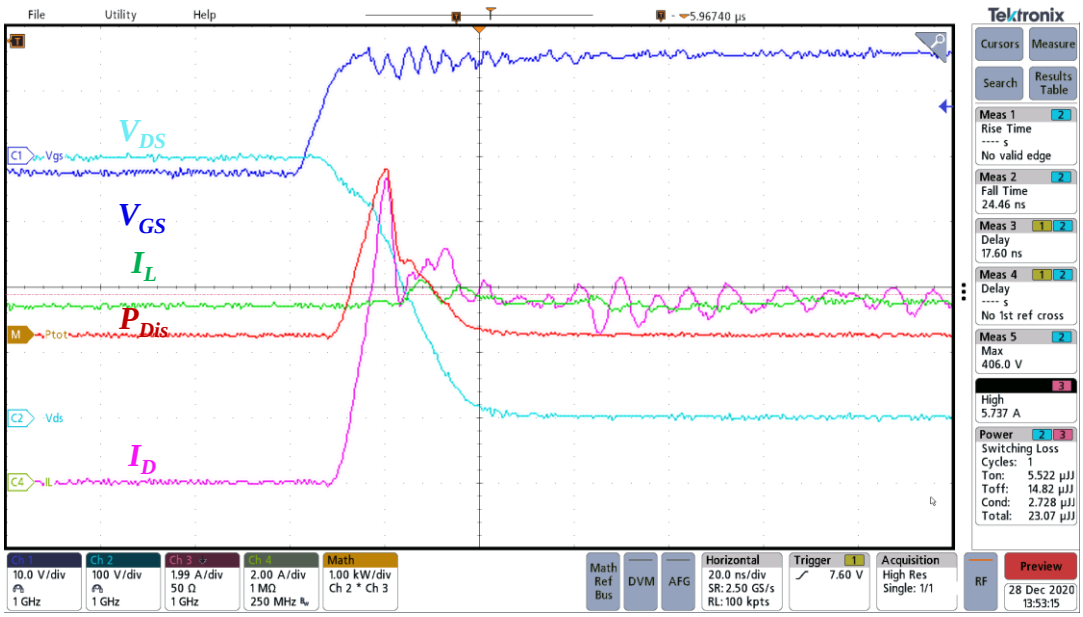

Fig. 42. Turn-on Transient of Double Pulse Test with FF06190A and 340µH Inductor

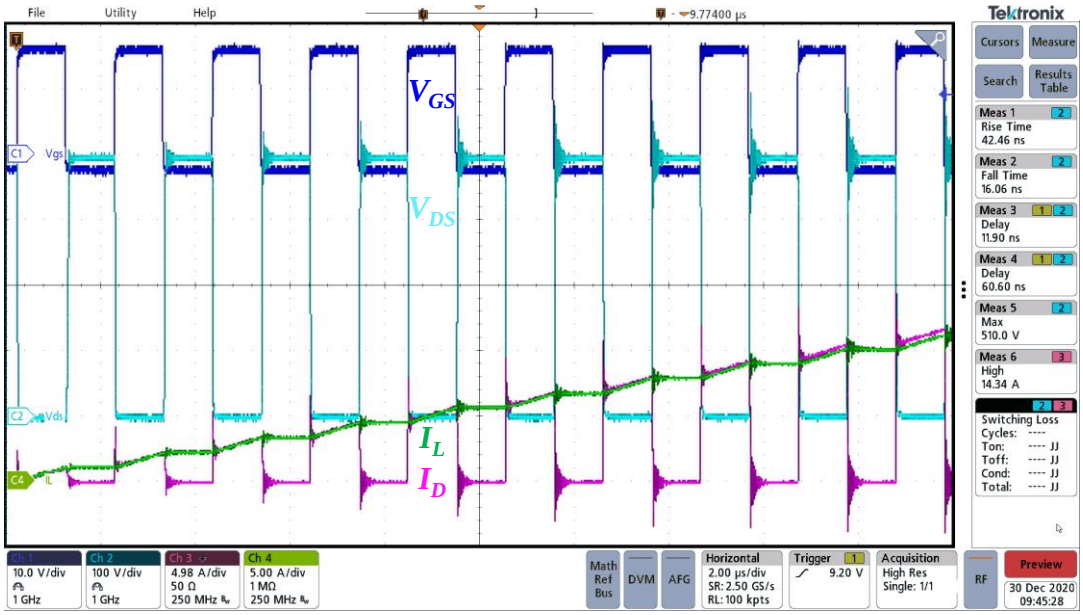

Fig. 43. Clamped Inductive Multi-pulse Switching with FF06190A and 340µH Inductor

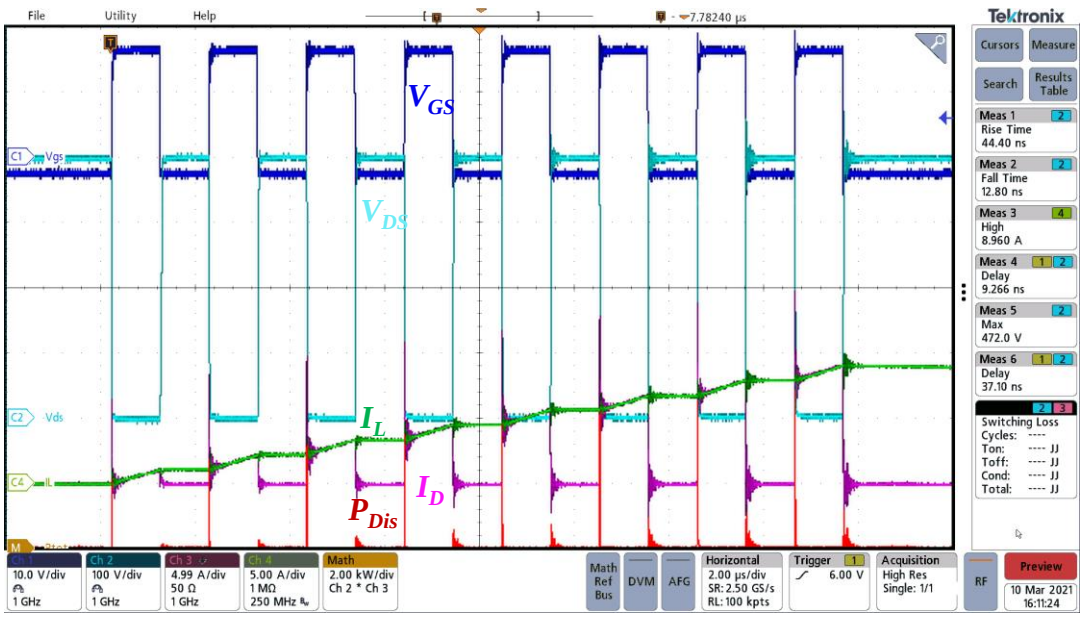

Fig. 44. Clamped Inductive Multi-pulse Switching with FF06370A and 340µH Inductor

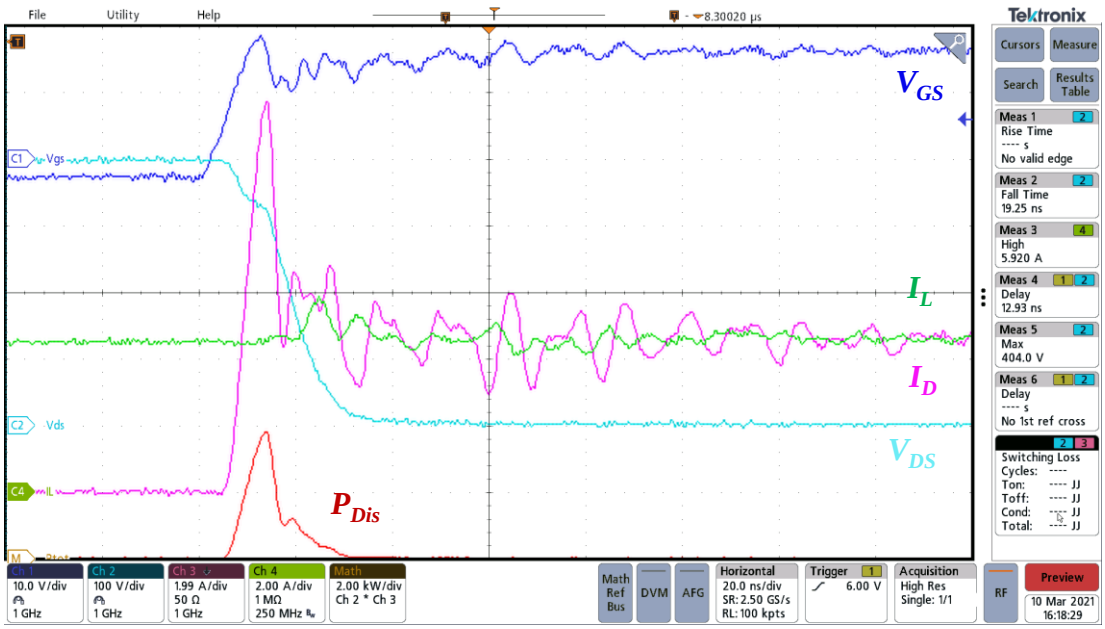

Fig. 45. Turn-on Transition of Clamped Inductive Switching with FF06370A @ 4.6A

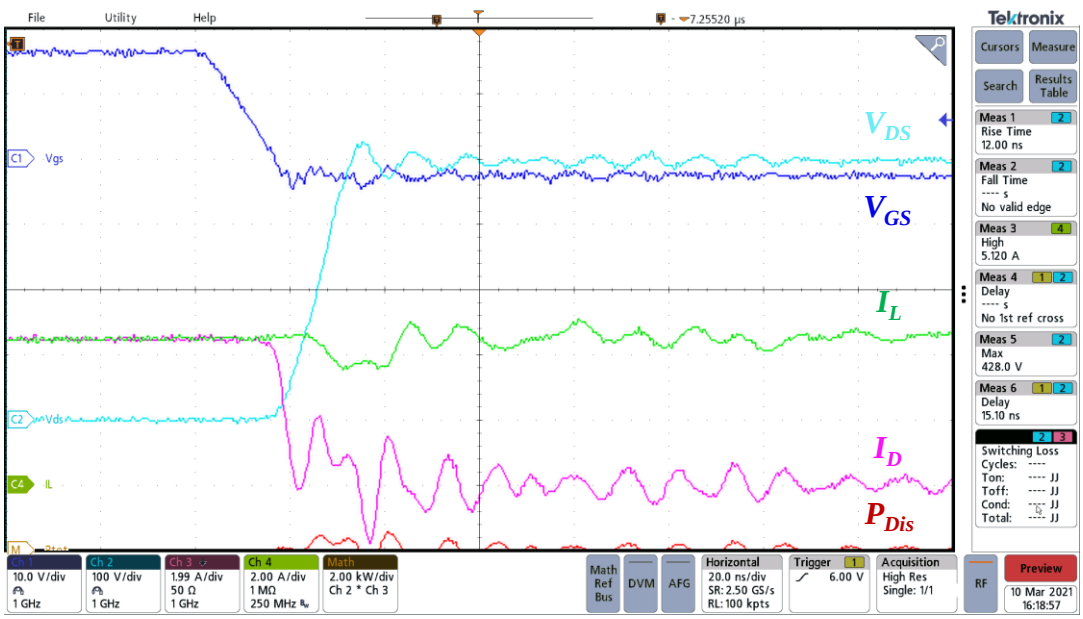

Fig. 46. Turn-off Transition of Clamped Inductive Switching with FF06370A @ 4.6A

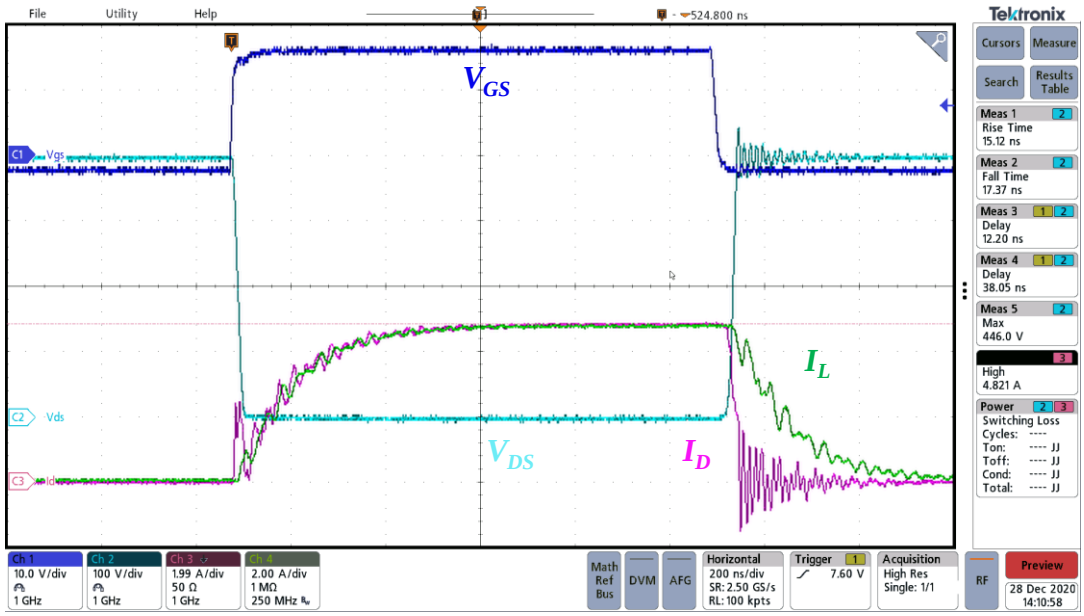

Fig. 47. Resistive Switching Waveform with FF06190A and 82Ω Resistor

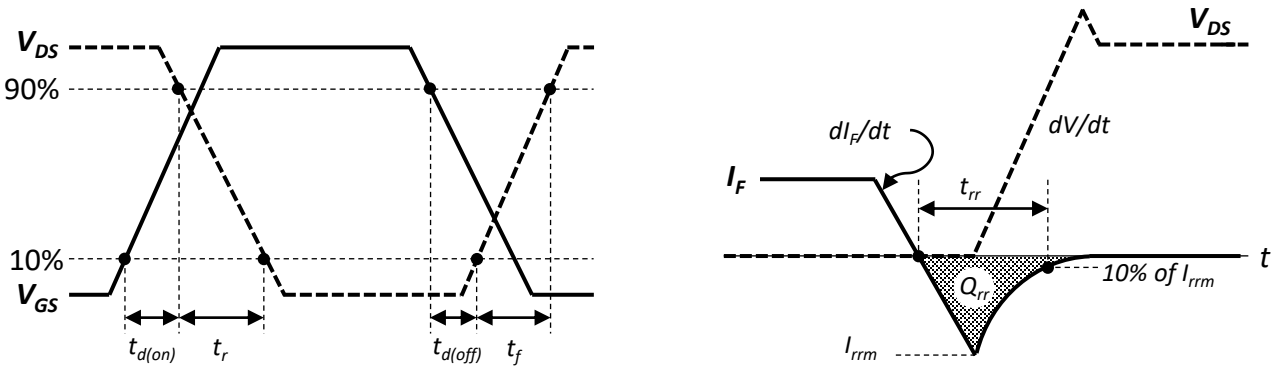

Fig. 48. Definition of Significant Dynamic Parameters

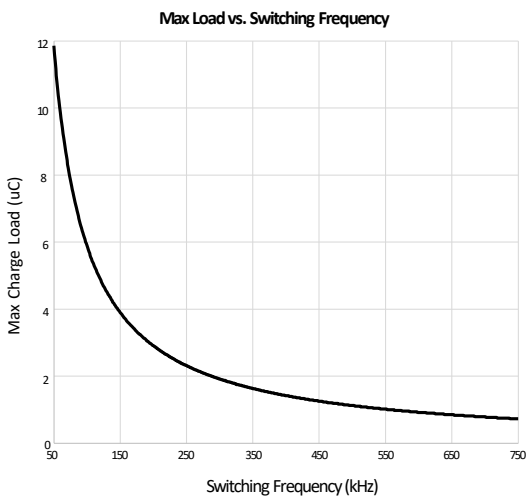

Fig. 49. Max Gate Charge Load vs. Max Switching Frequency of FSSEVB_GDrv

6. Document Information:

6.1 Revision History

Date	Revision	Changes
2021.5	A	1st issue

6.2 Important Note (Disclaimer)

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