FF12014M2

Product Datasheet

Silicon Carbide MOSFET

1200V, 13mΩ SiC MOSFET – Falcon Series

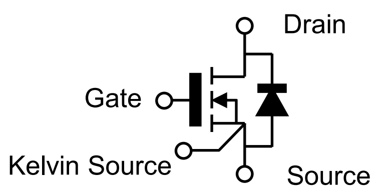
Features

- Optimized $R_{DS(on)}$ with Rapid Switching Behavior
- Compatible with Standard Gate Drivers
- Clean Kelvin-Source Switching Pin-out
- High Avalanche Endurance Capability
- Optimized for High Power Density Applications
- RoHS Compliant and Halogen Free

Potential Applications

- Switching Mode Power Supply
- PFC & DC/DC Converter
- EV Charging Station
- UPS
- Renewable Energy
- Power Inverter & Motor Driver

Product Information:



Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Enable High Temperature Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems
- High Reliability

Product Information	Packaging Type	
	QDPAK	T2PAK
Gate	1	1
Drain	12-22, Tab	Tab
Source	3-11	3-7
Kelvin Source	2	2
Part Number	FF12014M2L	FF12014M2T
Marking	FF12014M2	FF12014M2
Continuous Drain Current	127 A*	127 A*

Key Performance Parameters

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS} @$T_{j(max)}$	1200	V
Recommended Gate-Source Turn-On Voltage	V_{GS}	18	
Drain-Source On-State Resistance	$R_{DS(on)}$	13	mΩ
Continuous Drain Current	I_D	127	A
Pulse Drain Current	$I_{D,\ pulse}$	478	
Power Dissipation	P_{tot}	555	W
Avalanche Energy	E_{AS}	2700	mJ
Gate Charge	Q_G	382	nC
Output Capacitive Charge	Q_{oss}	290	
Junction & Storage Temperature	T_j, T_{stg}	-55 to 175	°C

For further information about comparable products, please contact (www.fastsic.com).

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Maximum Ratings: (T_j = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Voltage	V_{DSS}	1200	--	--	V	V_{GS}=0V, I_D=100μA
Continuous Drain Current*	I_D	--	127 91	--	A	V_{GS}=18V, T_C=25°C V_{GS}=18V, T_C=100°C
Pulse Drain Current*	$I_{D, pulse}$	--	478	--	A	t_{pulse} limited by $T_{j,max}$
Continuous Body Diode Currentμm*	I_S	--	96	--	A	V_{GS}=0V, T_C=25°C
Avalanche Energy, Single Pulse*	E_{AS}	--	2700	--	mJ	L=25mH
Operate Gate Source Voltage	$V_{GS, op}$	-10~0	--	15~18	V	Recommended operating values
Transient Gate Source Voltage	$V_{GS, tran.}$	-12	--	21	V	Transient operating limit (AC f > 1Hz, pulse width < 100ns)
Power Dissipation*	P_{tot}	--	555	--	W	T_c=25°C
Junction Temperature	T_j	-55	--	175	°C	--
Storage Temperature	T_{stg}	-55	--	175	°C	--
Soldering Temperature	T_L	--	--	260	°C	--
Junction Temperature	$T_{j,ext}$	-55	--	200	°C	t <100 hours

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
DC Characteristics (at T_j = 25°C, unless otherwise specified)						
Drain-source Breakdown Voltage	$V_{(BR)DSS}$	1200	--	--	V	V_{GS}=0V, I_D=100μA, T_j=25°C
Drain-Source On-State Resistance	$R_{DS(on)}$	--	12.4 13.8	--	mΩ	V_{GS}=18V, I_D=50A, T_j=25°C V_{GS}=15V, I_D=50A, T_j=25°C
Gate-Source Threshold Voltage	V_{th}	--	2.5	--	V	V_{GS}=V_{DS}, I_D=100mA
Zero Gate Voltage Drain Current	I_{DSS}	--	1	100	μA	V_{DS}=1200V, V_{GS}=0V, T_j=25°C
Gate-Source Leakage Current	I_{GSS}	--	--	100	nA	V_{GS}=18V, V_{DS}=0V
Body Diode Forward Voltage	V_{SD}	-- --	2.8 2.5	-- --	V	V_{GS}=0V, I_S=30A, T_j=25°C V_{GS}=0V, I_S=30A, T_j=100°C
AC Characteristics (at T_j = 25°C, unless otherwise specified)						
Input Capacitance	C_{iss}	--	7653	--	pF	V_{DS}=800V, V_{GS}=0V, f=250kHz, V_{AC}=25mV
Output Capacitance	C_{oss}	--	203	--	pF	
Reverse Capacitance	C_{rss}	--	9.7	--	pF	
Effective Output Capacitance, energy related	$C_{o(er)}$[1]	--	241	--	pF	
Effective Output Capacitance, time related	$C_{o(tr)}$[2]	--	337	--	pF	
C_{oss} Stored Energy	E_{oss}	--	81.6	--	μJ	
Output Capacitive Charge	Q_{oss}	--	290	--	nC	
Internal Gate Resistance	$R_{G, int.}$	--	1.5	--	Ω	f=1MHz, V_{AC}=25mV

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 800V.
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 800V.

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Switching Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Characteristics						
Gate to Source Charge	Q_{GS}	--	68	--	nC	V_{DS}=800V, V_{GS}=0V/18V, I_D=50A
Gate to Drain Charge	Q_{GD}	--	146	--		
Total Gate Charge	Q_G	--	382	--		

Thermal Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal Impedance, junction-case	$R_{th\text{-}jc}$	--	0.20			QDpak
		--	0.20	--		T2PAK
Thermal Impedance, junction-ambient	$R_{th\text{-}ja}$	--	40	--		Device on PCB, with 6 cm² of cooling area

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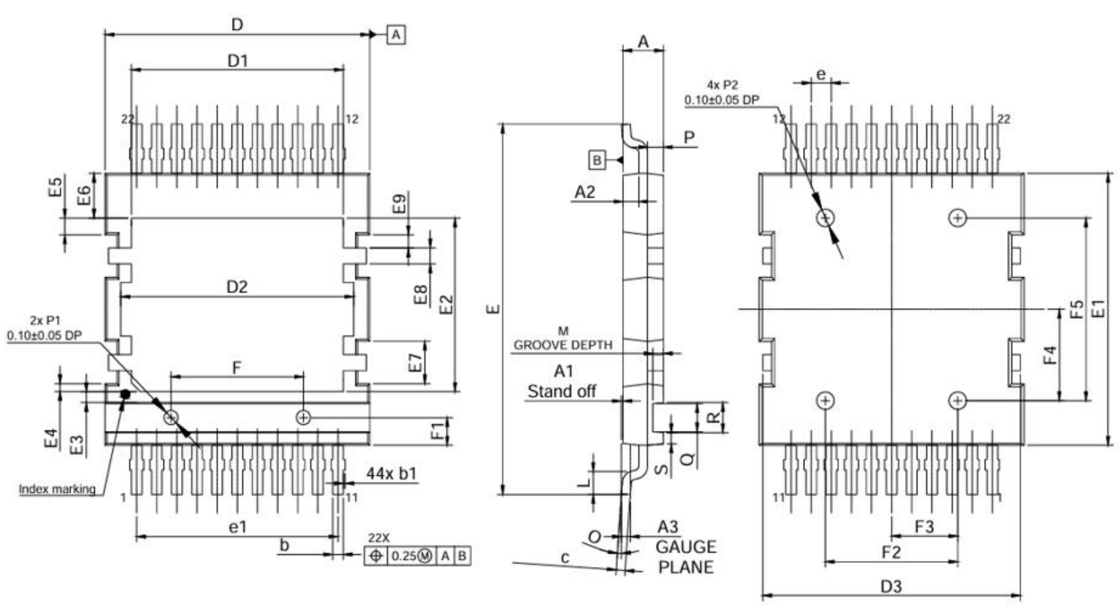
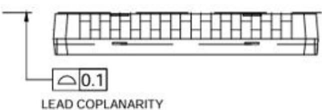
Package Outline (QDPAK)





SYMBOL	MIN	TYP	MAX	SYMBOL	MIN	TYP	MAX
A	2.25	2.3	2.35	E9		0.75	
A1	0	0.075	0.15	e		1.14	
A2		0.9		e1		11.4	
A3		0.5		F	7.4	7.5	7.6
b	0.5	0.6	0.7	F1	1.47	1.57	1.67
b1	--	0.15	0.15	F2	7.4	7.5	7.6
c	0.46	0.52	0.58	F3	3.65	3.75	3.85
D	14.9	15	15.1	F4	5.07	5.17	5.27
D1		12		F5	10.24	10.34	10.44
D2		13.2		L		1.3	
D3	14.5	14.6	14.7	M		0.6	
E	20.81	20.96	21.11	N		22	
E1	15.3	15.4	15.5	O	0°	--	8°
E2		9.83		P		0.9	
E3		0.625		P1	0.7	0.8	0.9
E4		0.45		P2	0.9	1	1.1
E5		0.95		Q		1.6	
E6		2.53		R		1.7	
E7		2.4		S		0.631	
E8		0.9					

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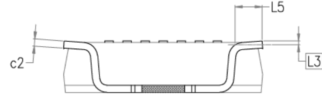
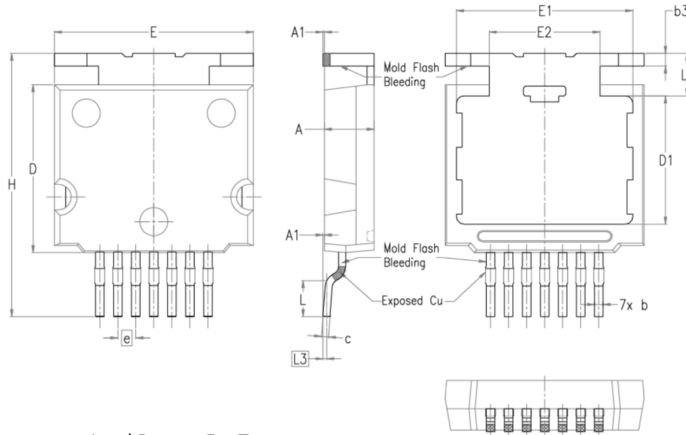
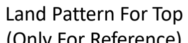
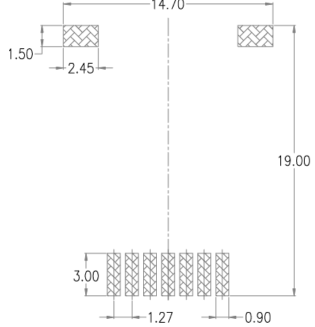
Package Outline (T2PAK)





Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	3.40	3.50	3.60
A1	0.00	0.10	0.25
b	0.50	0.60	0.70
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	9.00	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e	1.27 BSC		
H	18.00	18.50	19.00
L	2.30	2.50	2.75
L1	--	3.05	--
L3	--	0.26	--
L5	1.70	1.90	2.15





Note:

1. All dimension are in mm.
2. Dimension D & E do not include mold flash. Mold flash shall not exceed 0.127mm per side. These dimensions are measured at the outermost extreme of the plastic body.
3. Thermal pad contour optional within dimensions L1, D1 & E1.
4. Dimension D1 & E1 establish a minimum mounting surface for the thermal pad.
5. ▩ is exposed copper.

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Revision History

Date	Revision	Changes
2026.01	Tentative	First issue.

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