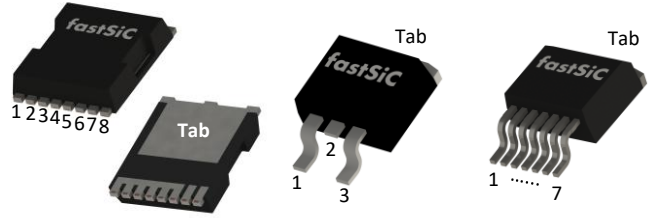
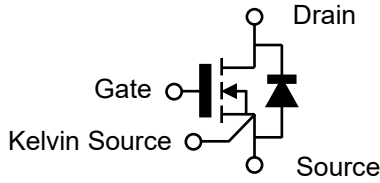


Silicon Carbide MOSFET

650V, 65mΩ SiC MOSFET – Falcon Series



Product Information:



TOLL

TO-263-3L

TO-263-7L

Features

- Optimized $R_{DS(on)}$ with Rapid Switching Behavior
- Compatible with Standard Gate Drivers
- Clean Kelvin-Source Switching Pin-out (Optional)
- High Avalanche Endurance Capability
- Optimized for High Power Density Applications
- RoHS Compliant and Halogen Free

Terminal	Packaging Type		
	TOLL	TO-263-3L	TO-263-7L
Gate	1	1	1
Drain	Tab	2, Tab	Tab
Source	3-8	3	3, 4, 5, 6, 7
Kelvin Source	2	--	2

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Enable High Temperature Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems
- High Reliability

Potential Applications

- Switching Mode Power Supply
- PFC & DC/DC Converter
- Portable Adaptor
- EV On Board Charger
- Renewable Energy
- Power Inverter & Motor Driver

Key Performance Parameters

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS @ T_{j(max)}}$	700	V
Recommended Gate-Source Turn-On Voltage	V_{GS}	12~18	
Drain-Source On-State Resistance	$R_{DS(on)}$	65	mΩ
Continuous Drain Current	I_D	20	A
Pulse Drain Current	$I_{D, pulse}$		
Power Dissipation	P_{tot}	175	W
Avalanche Energy	E_{AS}	250	mJ
Gate Charge	Q_G	27.8	nC
Output Capacitive Charge	Q_{oss}	30.4	
Junction & Storage Temperature	T_j, T_{stg}	-55 to 175	°C

Part Number	Package	Marking
FF06080M2F	TOLL	FF06080M2
FF06080M2J	TO-263-3L	FF06080M2
FF06080M2J-7	TO-263-7L	FF06080M2

For further information about comparable products, please contact (www.fastsic.com).

Maximum Ratings: ($T_j = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Voltage	V_{DSS}	650	--	--	V	$V_{GS}=0\text{V}, I_D=1\text{mA}$
Continuous Drain Current	I_D	--	20 10	--	A	$V_{GS}=15\text{V}, T_c=25^\circ\text{C}$ $V_{GS}=15\text{V}, T_c=100^\circ\text{C}$
Pulse Drain Current	$I_{D,pulse}$	--	TBD	--		Per SOA
Continuous Body Diode Current	I_S	--	15	--		$V_{GS}=0\text{V}, T_c=25^\circ\text{C}$
Avalanche Energy, Single Pulse	E_{AS}	--	--	250	mJ	$L=25\text{mH}$
Operate Gate Source Voltage	$V_{GS,op}$	-8~0	--	12~18	V	Recommended operating values
Transient Gate Source Voltage	$V_{GS,tran.}$	-9	--	19		Transient operating limit ($AC f > 1\text{Hz}$, pulse width $< 100\text{ns}$)
Power Dissipation	P_{tot}	--	175	--	W	$T_c=25^\circ\text{C}$
Power Dissipation	P_{tot}	--	65	--		$T_c=25^\circ\text{C}$
Junction Temperature	T_j	-55	--	175	°C	--
Storage Temperature	T_{stg}	-55	--	175		
Soldering Temperature	T_L	--	--	260		

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
DC Characteristics (at $T_j = 25^\circ\text{C}$, unless otherwise specified)						
Drain-source Breakdown Voltage	$V_{(BR)DSS}$	650	--	--	V	$V_{GS}=0\text{V}, I_D=1\text{mA}, T_j=25^\circ\text{C}$
Drain-Source On-State Resistance	$R_{DS(on)}$	--	94 75 65	--	mΩ	$V_{GS}=12\text{V}, I_D=8\text{A}, T_j=25^\circ\text{C}$ $V_{GS}=15\text{V}, I_D=8\text{A}, T_j=25^\circ\text{C}$ $V_{GS}=18\text{V}, I_D=8\text{A}, T_j=25^\circ\text{C}$
Gate-Source Threshold Voltage	V_{th}	--	2.5	--	V	$V_{GS}=V_{DS}, I_D=8\text{mA}$
Zero Gate Voltage Drain Current	I_{DSS}	--	1	1000	μA	$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$
Gate-Source Leakage Current	I_{GSS}	--	--	100	nA	$V_{GS}=15\text{V}, V_{DS}=0\text{V}$
Body Diode Forward Voltage	V_{SD}	--	2.65 2.45	--	V	$V_{GS}=0\text{V}, I_S=4\text{A}, T_j=25^\circ\text{C}$ $V_{GS}=0\text{V}, I_S=4\text{A}, T_j=175^\circ\text{C}$
AC Characteristics (at $T_j = 25^\circ\text{C}$, unless otherwise specified)						
Input Capacitance	C_{ISS}	--	1030	--	pF	$V_{DS}=400\text{V}, V_{GS}=0\text{V},$ $f=250\text{kHz}, V_{AC}=25\text{mV}$
Output Capacitance	C_{OSS}	--	48	--		
Reverse Capacitance	C_{RSS}	--	3.2	--		
Effective Output Capacitance, energy related	$C_{o(er)}^1$	--	65	--		
Effective Output Capacitance, time related	$C_{o(tr)}^2$	--	85	--		
C_{OSS} Stored Energy	E_{OSS}	--	4	--		
Output Capacitive Charge	Q_{OSS}	--	30.4	--	nC	
Internal Gate Resistance	$R_{G,int.}$	--	5.5	--	Ω	$f=1\text{MHz}, V_{AC}=25\text{mV}$

¹ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400V.

² $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400V.

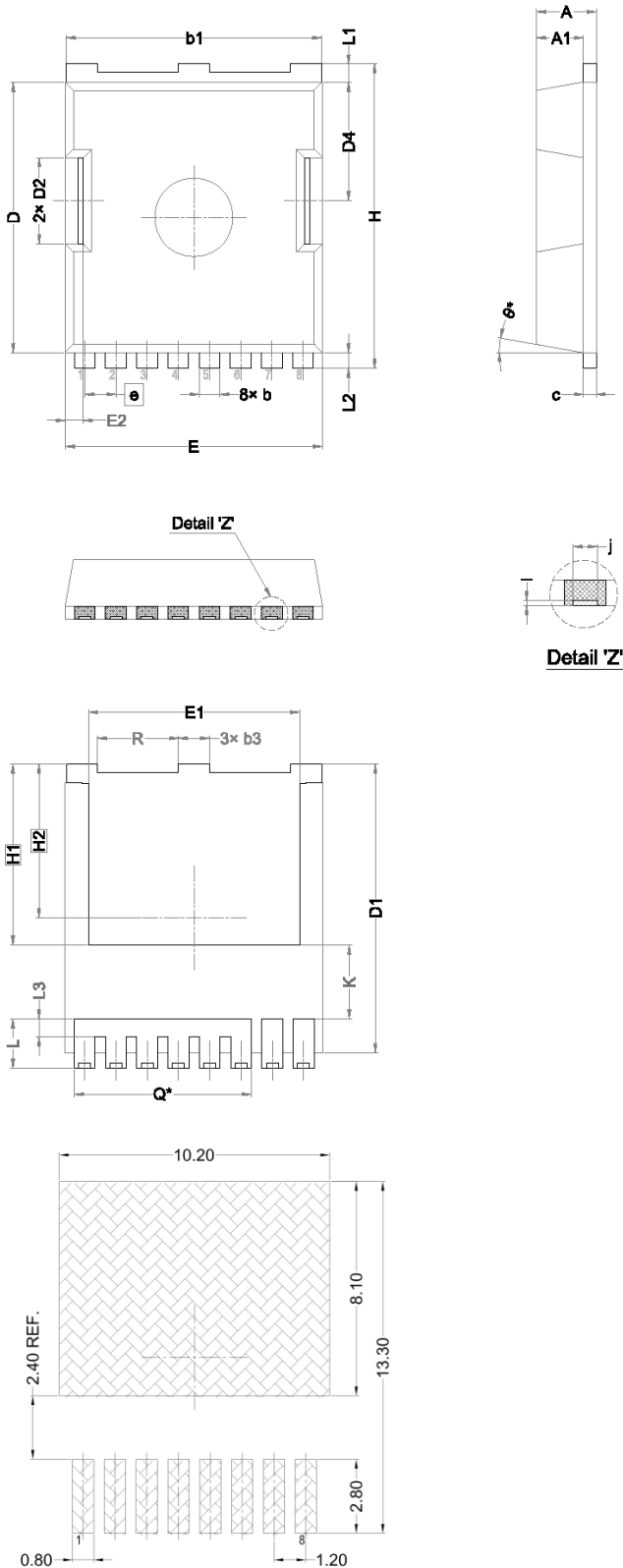
Switching Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Characteristics						
Gate to Source Charge	Q_{GS}	--	7.4	--	nC	$V_{DS}=400V, V_{GS}=0V/15V, I_D=8A$
Gate to Drain Charge	Q_{GD}	--	8.3	--		
Total Gate Charge	Q_G	--	27.8	--		
Turn On Delay Time	$t_{d(on)}$	--		--	ns	$V_{DS}=400V,$ $I_D=8A,$ $V_{GS}=-3/+15V,$ $R_{G, ext.} = 4.7\Omega$ FWD=Self
Rise Time	t_r	--		--		
Turn Off Delay Time	$t_{d(off)}$	--		--		
Fall Time	t_f	--		--		
Turn On Switching Energy	E_{on}	--	40	--	μJ	
Turn Off Switching Energy	E_{off}	--	6	--		
Body Diode Characteristics						
Reverse Recovery Charge	Q_{rr}	--	46.2	--	nC	$V_{GS}=0V,$ $I_S=8A, V_{DS}=400V,$ $di/dt=-A/\mu s$ * Q_{rr} herein excluded the Q_{oss} value.
Reverse Recovery Time	t_{rr}	--		--	ns	
Peak Reverse Recovery Current	I_{rrm}	--		--	A	

Thermal Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal Impedance, junction-case	R_{th-jc}	--	0.85	--	K/W	JESD-51-14
Thermal Impedance, junction-ambient	R_{th-ja}	--	40	--		Device on PCB, with 6 cm ² of cooling area

Package Outline (TOLL, MO-299B)



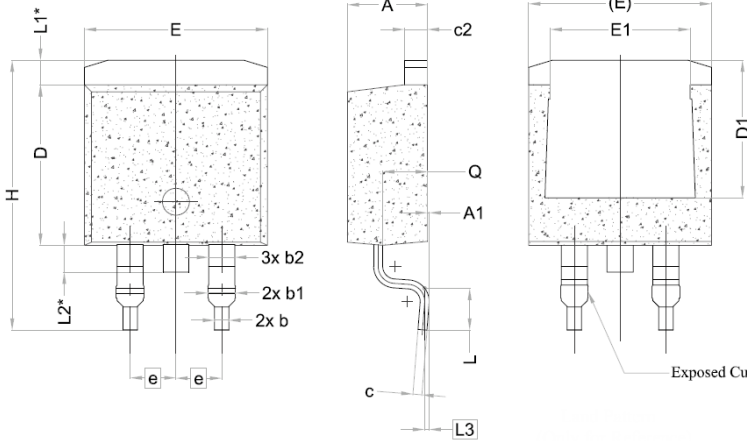
Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	8.00	8.10	8.20
E2	0.60	0.70	0.80
e	1.20 BSC.		
H	11.58	11.68	11.78
H1	6.95 BSC.		
H2	5.89 BSC.		
i	0.10 REF.		
j	0.46 REF.		
K	2.80 REF.		
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	0.80
N	8		
Q	6.80 REF.		
R	3.00	3.10	3.20
θ	10° REF.		

Note:

1. Dimensions do not inclusive burrs and mold flash.
2. "*" is for reference.

Land Pattern (Only for reference)

Package Outline (TO-263-3L, D2PAK)

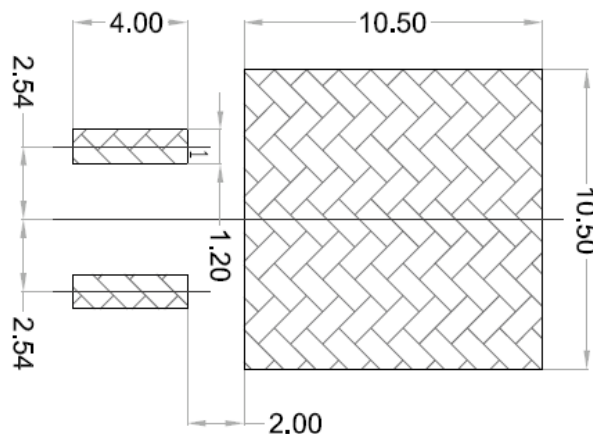


Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	4.24	4.44	4.64
A1	0.00	0.10	0.25
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
c2	1.15	1.27	1.40
D	8.82	8.92	9.02
D1	6.86	7.65	--
E	9.96	10.16	10.36
E1	6.89	7.77	7.89
e	2.54 BSC		
H	14.61	15.00	15.88
L	1.78	2.32	2.79
L1	1.36 REF.		
L2	1.50 REF.		
L3	0.25 BSC		
Q	2.30	2.48	2.70

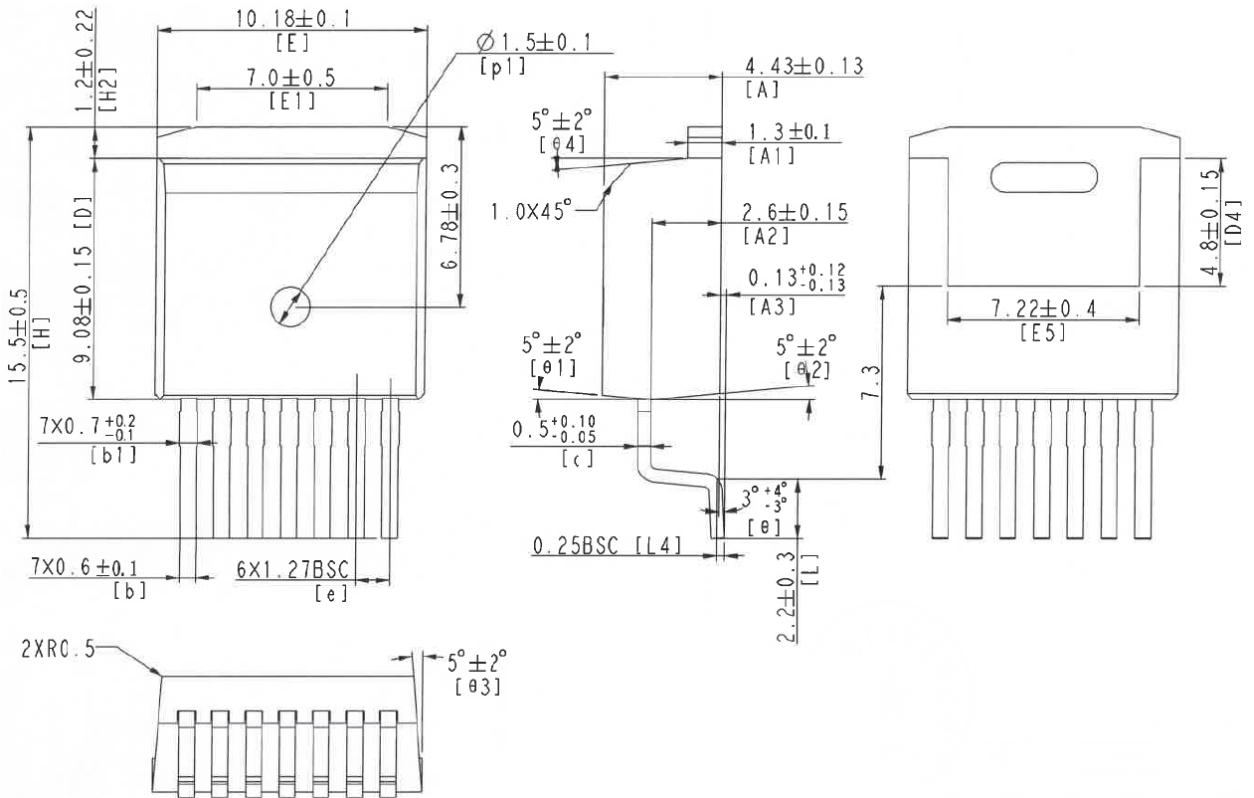
Note:

1. All dimensions are in mm.
2. Dimension D & E do not include mold flash. Mode flash shall not exceed 0.127mm per side. These dimensions are measured at the outermost extreme of the plastic body.
3. Thermal pad contour optional within dimensions E, L1, D1 & E1.
4. Dimension D1 & E1 establish a minimum mounting surface for the thermal pad.
5. "*" is reference.

Land Pattern (Only for Reference)



Package Outline (TO-263-7L)



Revision History

Date	Revision	Changes
2026.03	Tentative	First issue. All data is the target spec.

Important Note (Disclaimer)

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